IQ-LinkUART – Frame-based wrapper for the UART

Description

IQ-LinkUART is a frame-based wrapper for the UART interface. It is designed to receive frames containing commands for the bus operations and the wrapper configuration.

All frames are confirmed by an answering frame. The commands are identified by a 3-bit tag, and all frames are protected from error by a 16-bit CRC (CCITT).

IQ-LinkUART doesn't check for the compatibility with the system bus, so the UART controller should send only commands which conform to the bus specification.

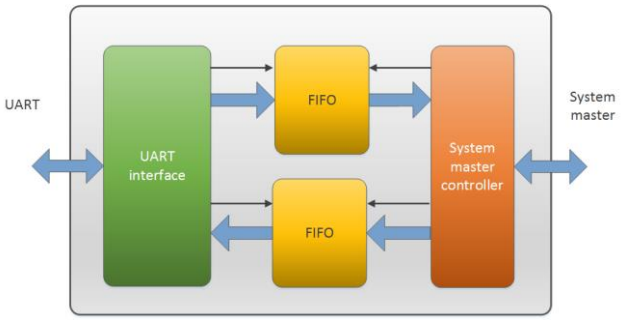
Applications

- Vending machines
- Video monitors
- Human machine interface (HMI) systems
- Industrial control and monitoring

Deliverables

- Encrypted RTL source code supporting SOPC builder (Altera) / Precompiled IP core in desired configuration (Lattice)
- Testbench
- Datasheet
- User manual
- Implementation guide

Block Diagram



Implementation

Altera Cyclone III (EP3C16)

LEs	BRAMs (M9K)	Multip.	F_{max}	IO Pins
956	2	0	169 MHz *	118 **

Lattice (ECP3-35EA)

LUT4s	Regs	EBRs	Multip.	F_{max}	IO Pins
963	449	2	0	174 MHz *	118 **

* Maximum frequency of the system bus interface, for AMBA AHB

** Assuming all core ports routed off-chip

Verification

The core has been rigorously tested in functional simulation and actual hardware.

The core is accompanied with an automated testbench with an UART simulation model and a memory simulation model.

The memory model can be initialized with the desired data using the standard memory initialization file.

Features

- Configurable UART bitrate (all standard and non-standard bitrates supported)
- Detection of errors using a 16-bit CRC (CCITT).
- Decoupled command and response interfaces, allowing for high efficiency of the communication.
- FIFO-based interface with configurable depth, allowing a trade-off between resource use and maximum number of commands issued before receiving responses.
- Easy adaptation to the various FPGAs and various design requirements (ranging from slow, low-budget interfaces to the high bandwidth applications)
- Integrated DMA memory master supporting low-overhead burst transfers
    - *Master bus interfaces*
        - *AMBA AHB*
        - *AMBA AXI4*
        - *Avalon*
        - *Peregrine**

* Peregrine bus is Mikroprojekt's proprietary bus architecture, optimized for FPGA architecture

Contact info

Mikroprojekt Ltd.
Aleja Blaža Jurišića 9
HR-10040 Zagreb
Croatia

tel/fax +385 1 2455 659

mail: contact@mikroprojekt.hr
web: http://www.mikroprojekt.hr