IQ-Mem – High Performance Memory Controller

Description

IQ-Mem is a high performance memory controller for SDRAM DDR memories. It is designed to offer memory access to the system bus masters with maximum efficiency and minimum resource consumption.

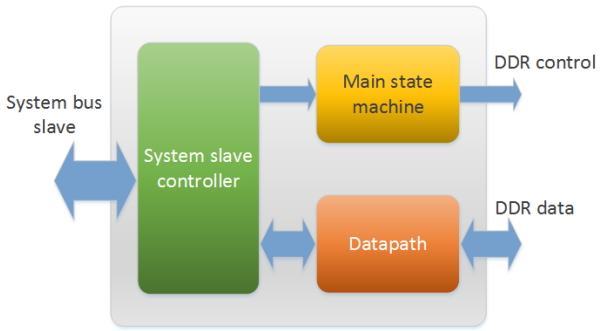
All memory architecture and timing parameters are configurable at compile time. IQ-Mem will automatically perform the memory initialization on start-up and the memory refresh during operation.

For systems requiring fast random access within a localized memory area, the IQ-Mem supports access acceleration by avoiding the issue of the PRECHARGE command. The last accessed SDRAM memory bank remains open, halving the access overhead, until the next refresh cycle or an access to a different bank.

Applications

- Vending machines
- Video monitors
- Automotive infotainment
- Medical instrumentation
- Human machine interface (HMI) systems
- Mobile devices

Block Diagram



Implementation

Altera Cyclone III (EP3C16)

LEs	BRAMs (M9K)	Multip.	F_{max}	IO Pins
2184	3	0	173 MHz *	160 **

Lattice (ECP3-35EA)

LUT4s	Regs	EBRs	Multip.	F_{max}	IO Pins
526	497	0	0	215 MHz *	160 **

* Maximum frequency of the system bus interface, for AMBA AHB

** Assuming all core ports routed off-chip

Deliverables

- Encrypted RTL source code supporting SOPC builder (Altera) / Precompiled IP core in desired configuration (Lattice)
- Testbench
- Datasheet
- User manual
- Implementation guide

Verification

The core has been rigorously tested in functional simulation and actual hardware. The core is accompanied with an automated testbench with a system bus master simulation model and a memory simulation model. The memory model is provided by the memory manufacturer, it will report errors during simulation.

Features

- Configurable memory architecture (address width, data width, number of chip selects)
- Configurable timing parameters and CAS latency (at core compile time)
- Support for SDRAM, DDR, DDR2 and DDR3 memories
- Pre-configured proven timing setups for various memory vendors
- Option for powering down external memory (auto-refresh mode) to lower power consumption
- Option for avoiding the PRECHARGE command to keep banks open and reduce access latency
- High-throughput design
- Integrated system bus slave supporting low-overhead burst transfers
    - Slave bus interfaces
        - *AMBA AHB*
        - *AMBA AXI4*
        - *Avalon*
        - *Peregrine**

* Peregrine bus is Mikroprojekt's proprietary bus architecture, optimized for FPGA architecture

Contact info

Mikroprojekt Ltd.
Aleja Blaža Jurišića 9
HR-10040 Zagreb
Croatia

tel/fax +385 1 2455 659

mail: contact@mikroprojekt.hr
web: http://www.mikroprojekt.hr