IQ-DispML - Multi-layer Configurable Display Controller

Description

The IQ-DispML is a multi-layer, fully software configurable display controller IP core. It performs continuous refresh of graphical flat panel displays (TFT LCD, AMOLED) from the designated frame buffers located in a memory device mapped to the system bus. Multiple layers are blended into a single image, which is outputted to the display. SDRAM and SRAM devices are supported as frame buffers, depending on the bandwidth requirements.

IQ-DispML is designed to provide an optimum tradeoff of performance and resource utilization in FPGA devices while retaining a high degree of configurability.

The IP core can be additionally scaled down at compile time by reducing the number of layers, bus widths and fixing timing parameters, allowing the user to fully optimize the IQ-DispML for a specific configuration

Applications

- Vending machines
- Video monitors
- Automotive infotainment
- Medical instrumentation
- Human machine interface (HMI) systems
- Mobile devices

Implementation

Lattice (ECP3-35EA)

Light version (2 layers, 32-bit pipeline)

LUT4s	Regs	EBRs	Multip.	F_{max}	IO Pins
4978	3018	4	9	180 MHz *	249 **

Full version (4 layers, 32-bit pipeline)

LUT4s	Regs	EBRs	Multip.	F_{max}	IO Pins
8670	5241	6	21	182 MHz *	249 **

* Maximum frequency of the system bus interface, for AMBA AHB

** Assuming all core ports routed off-chip

Deliverables

- Encrypted RTL source code supporting SOPC builder (Altera) / Precompiled IP core in desired configuration (Lattice)
- Testbench
- Datasheet
- User manual
- Implementation guide

Verification

The core has been rigorously tested in functional simulation and actual hardware. The core is accompanied with an automated testbench with an image source simulation model and a memory simulation model.

The memory model can dump content to a file, allowing analysis of the simulation results through simple software provided with the model.

Features

- Fully programmable clock and timing control for flat panel displays with progressive scanning
- Support for resolutions up to 4096x4096
- Completely variable timing parameters, for standard or specific display resolutions
- Support for 8,16, 18 or 24 bit RGB output color depth
  - *8-bit RGB (3:3:2)*
  - *16-bit RGB (5:6:5)*
  - *18-bit RGB (6:6:6)*
  - *24-bit RGB (8:8:8)*
- Standard or multiplexed display data bus
- Display power control lines
- Interrupt generation on vertical sync for software synchronization
- Frame buffer management
  - *Double buffering to reduce image flicker*
  - *Variable frame buffer organization with software-configurable memory stripe*
  - *Image scroll via unconstrained frame buffer addressing*
  - *Frame buffer color depth support:*
    - *8 bit RGB (3:3:2)*
    - *16 bit RGB(5:6:5)*
    - *24 bit RGB(8:8:8)*
    - *32 bit ARGB(8:8:8:8)*
- Alpha blending of all layers, with per-layer additional transparency (“layer fading”)
- Independent positioning and dimensioning of all layers
- Compile-time configuration for reducing resource cost by fixing parameters
- Support for multiple clock domains to ease timing closure
- Integrated DMA memory master supporting low-overhead burst transfers
  - *Master bus interfaces*
    - *AMBA (AHB |AXI4)*
    - *Avalon*
    - *Peregrine**

* Peregrine bus is Mikroprojekt’s proprietary bus architecture, optimized for FPGA architecture

- Configuration bus slave interface with address-mapped registers
  - Slave bus interfaces
    - AMBA APB
    - Avalon

Feature highlights

Fully programmable timing control and data driving

IQ-DispML integrates a fully register – programmable timing controller capable of driving a TFT LCD display panel or a video signal source driver such as 7:1 LVDS, HDMI or SDI cable driver.

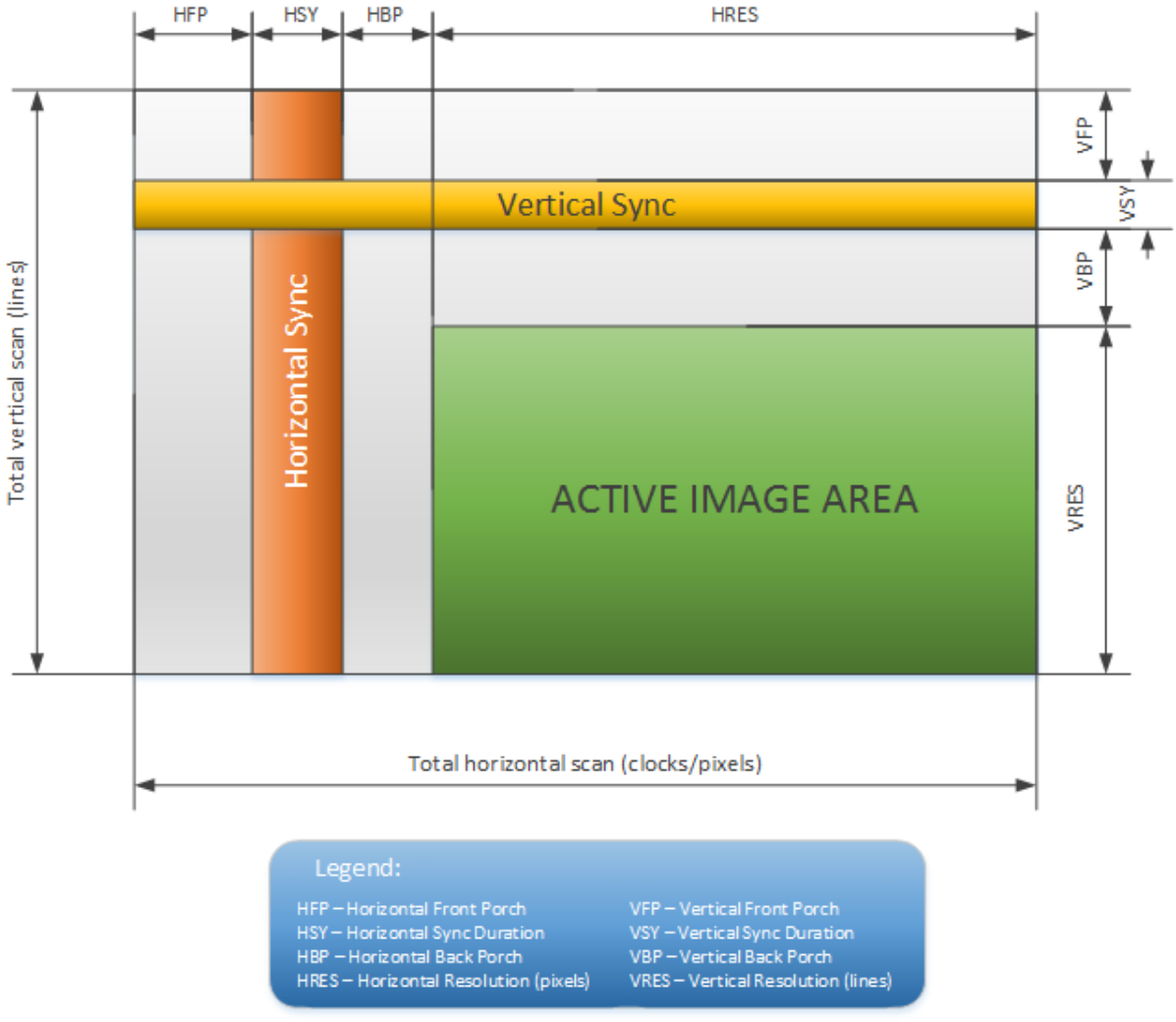

Figure 1: Programmable image scan

The pixel data is output as a parallel bus alongside standard timing signals: vertical sync (VSYNC), horizontal sync (HSYNC) and data valid/blanking (BLANK). The timing of these signals is fully programmable, supporting fully custom display timings as well as the standard VESA display timings. All timings are relative to the pixel clock signal which is input from an external programmable clock generator. All of the parameters (HSY, HFP, HBP, HRES, VSY, VFP, VBP, VRES) listed in Figure 1 are programmable and controllable through the IQ-DispML configuration registers.

Alongside the signal lines, IQ-DispML outputs separate control lines for the three-state buffers of output signals, as well as general purpose digital output lines usable for the power-up control of an external display or chip.

The IQ-DispML supports multiple output data formats. Whichever data format is used internally, it is mapped to the output format in the output datapath.

The following formats are supported in the output stage:

- 8-bit RGB (3:3:2)
- 16-bit RGB (5:6:5)
- 18-bit RGB (6:6:6)
- 24-bit RGB (8:8:8)

The entire output datapath is a separate clock domain decoupled from the system with a cross-clock FIFO conveying the pixel data.

Flexible memory organization

Images are usually stored in the memory as two-dimensional memory spaces of a certain size called frame buffers. Each frame buffer can contain one or more memory mapped digital images. The vertical distance between two pixels in a memory-mapped image is called stripe (or stride in some cases) and it defines the maximum size of an image line expressed in the number of bytes. The actual maximum resolution depends on the pixel mapping and the number of bytes allocated per pixel. Smaller images can be stored in the same space, yet the vertical distance between two pixels will remain one stripe.

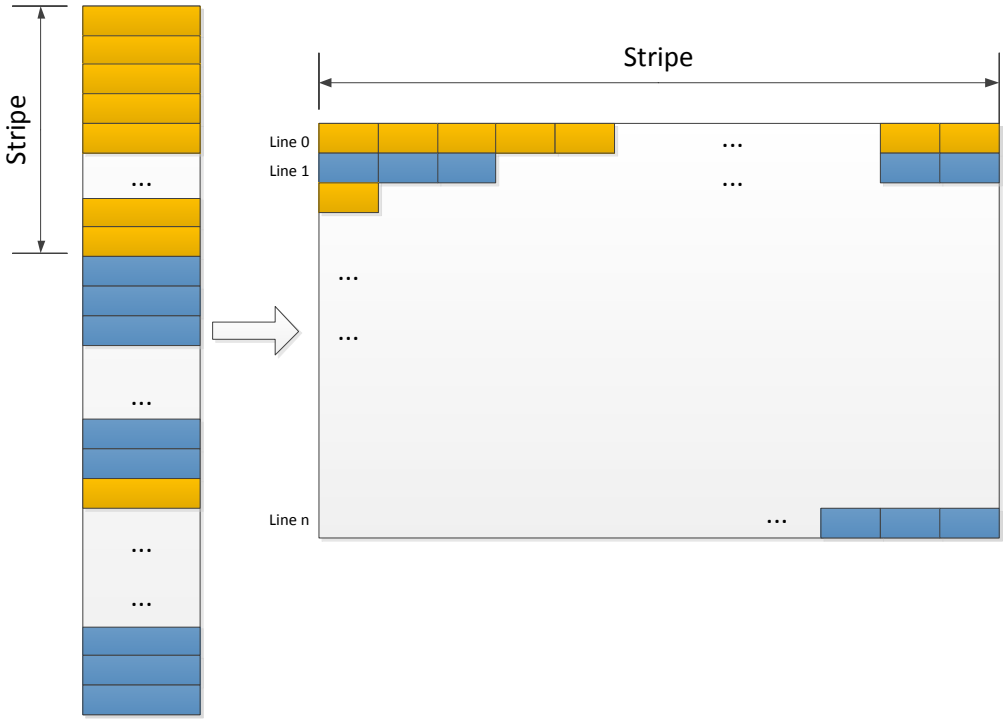

Figure 2: Frame buffer organization

The IQ-DispML integrates a programmable address generator which supports variable stripe settings at run-time, allowing the user to freely configure the memory mapping for the display image. The stripe can be of arbitrary size and can also be set negative, as required by the binary representation of various bitmap formats. A different stripe value can be adjusted for each of the image layers supported in the IQ-DispML.

For each of the image layers, a separate pixel mapping format can be set, defining the representation of the image in the memory.

- 8 bit RGB (3:3:2)
- 16 bit RGB(5:6:5)
- 24 bit RGB(8:8:8)
- 32 bit ARGB(8:8:8:8)

The image is fetched from a starting pixel address, defined as the position of the top-left pixel. The starting pixel address can be any address in the available memory space, and is dynamically programmable for each output frame via the configuration registers. This additionally allows for smooth scrolling effects on images, which can be scrolled frame by frame by changing the starting position of the viewed image. The programmable address generator automatically computes the stripe addition and the image fetch addresses to support scrolling in both dimensions.

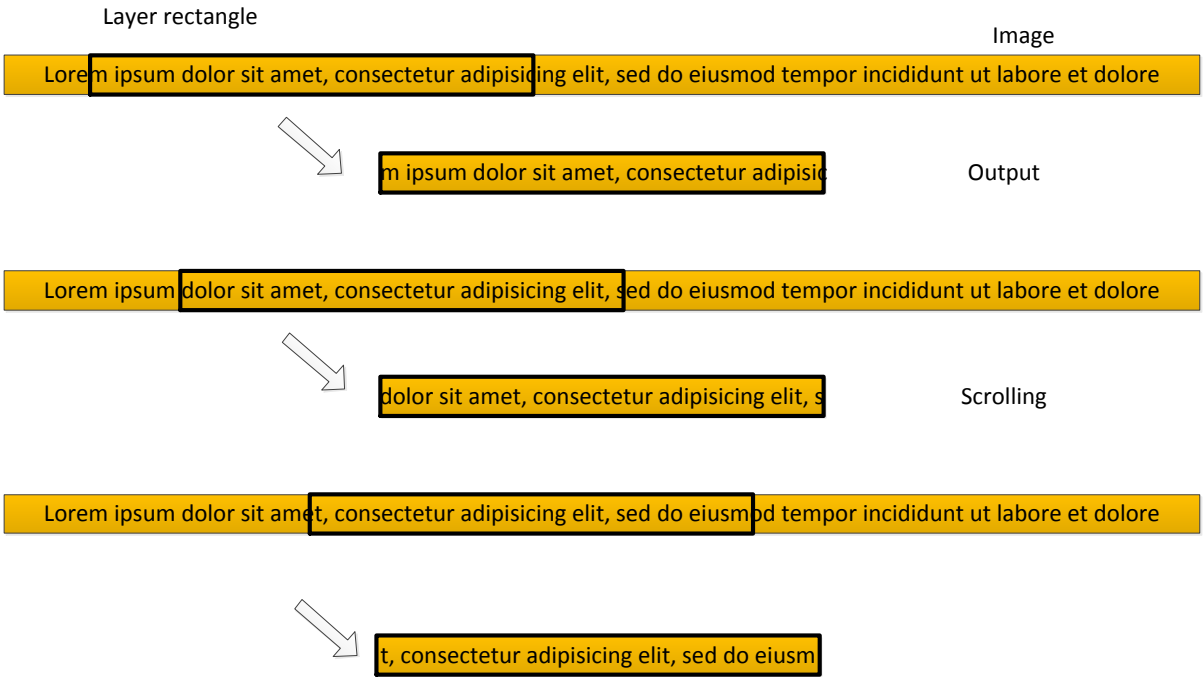

Figure 3: Smooth scrolling

žMulti-layer Alpha image compositing

IQ-DispML is a multilayer display controller capable of accessing multiple memory mapped images from different memory locations. Before outputting to the display, the images are combined in a single image by using alpha blending.

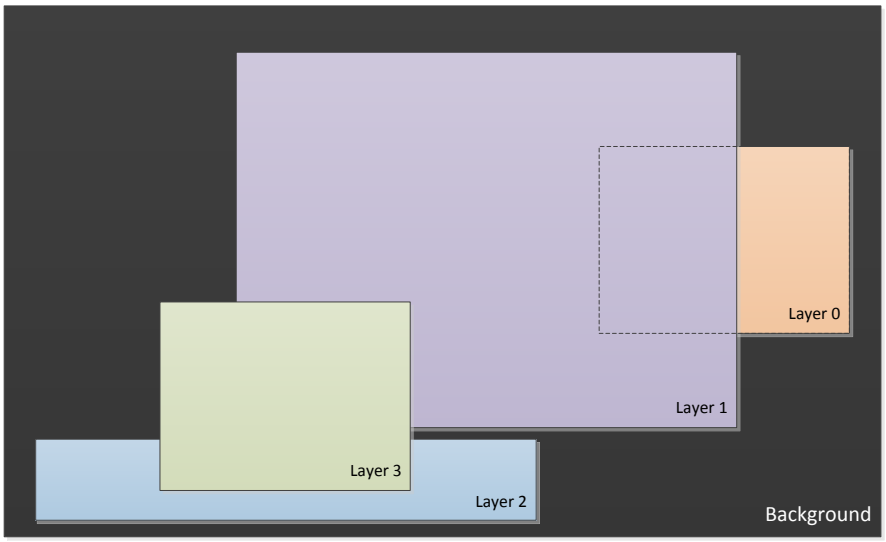

Figure 4: Layer stack

The output image size is defined by the output resolution of the connected display (HRES, VRES).

Within this viewing window, multiple layers are superimposed on a black background hierarchically:

- Layer 0 blends onto the black background
- Layer 1 blends onto black + Layer 0,
- Layer 2 blends onto black + Layer 0 + Layer 1…

The number of layers supported by the IQ-DispML can be defined at synthesis time. Each layer's image rectangle can be of arbitrary size (from 1x1 pixel to HRES x VRES) and can be positioned to an arbitrary position on within the output image (defined by its top left coordinate).

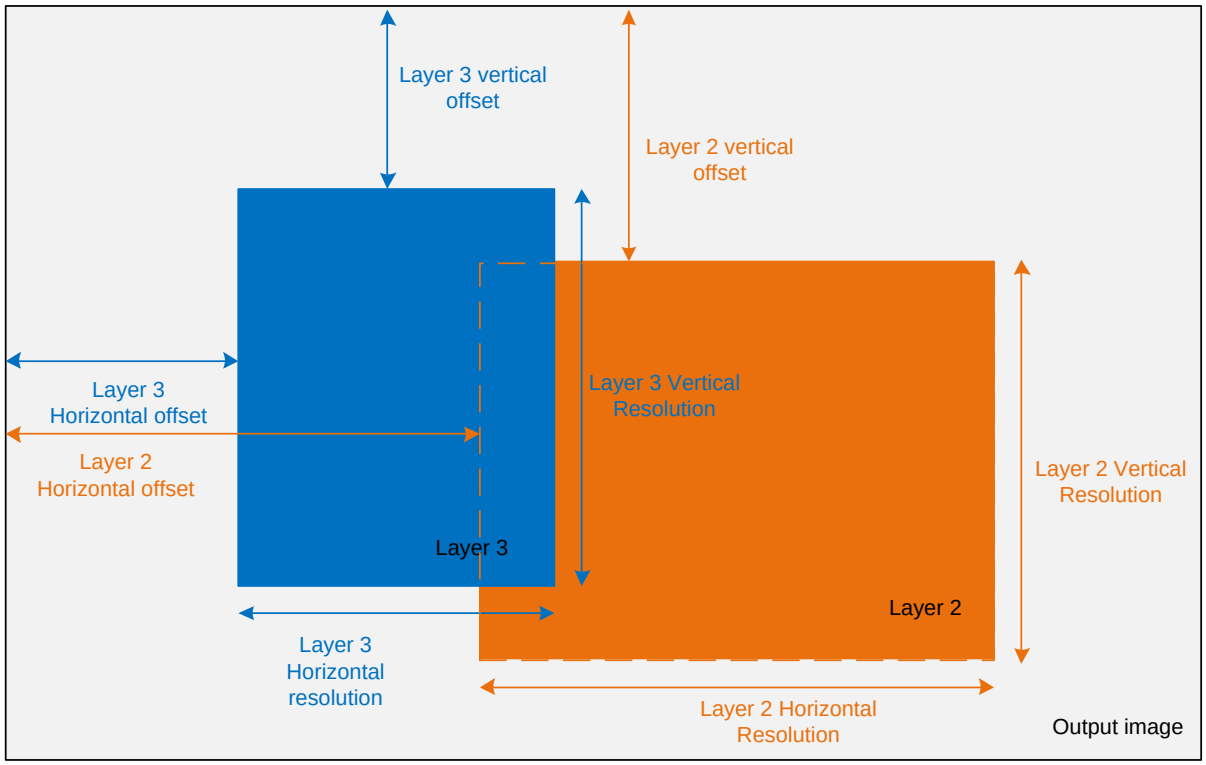

Figure 5: Layer positioning

The pixel format 32BPP ARGB allows the layered image to have a per-pixel transparency value of 0-255, allowing for precise translucency effects and antialiased edges on overlayed graphics. Additionally, each layer supports an additional overall transparency parameter (which stacks to the per-pixel transparency if present).

Figure 6: Mixing example

Detailed block schematic

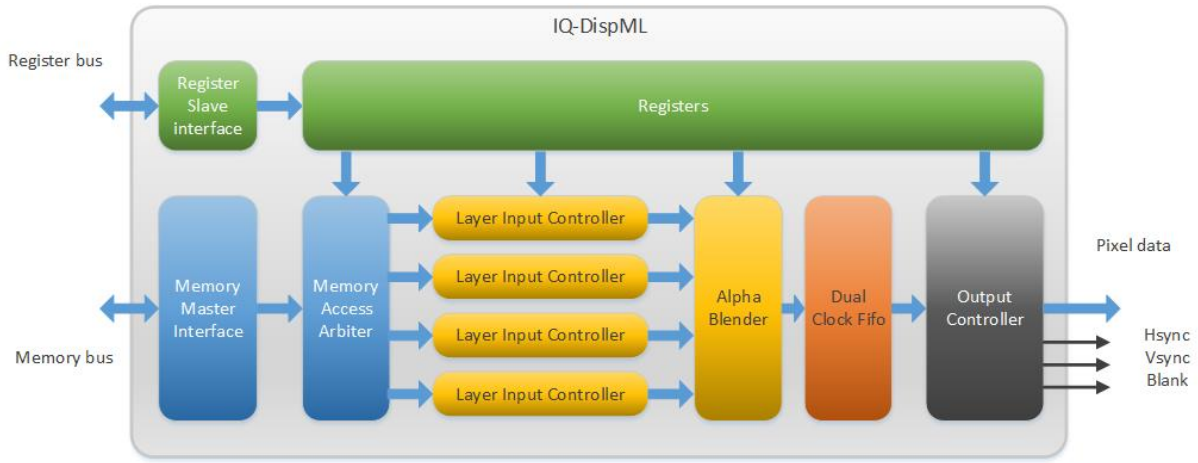

Figure 7: IQ-DispML Block diagram

In figure 7, the three colors (gray, orange, and blue) represent three independent clock domains in the IQ-DispML IP core.

Contact info

Mikroprojekt Ltd.
Aleja Blaža Jurišića 9
HR-10040 Zagreb
Croatia

tel/fax +385 1 2455 659
mail: contact@mikroprojekt.hr
web: http://www.mikroprojekt.hr