mikroprojekt

SDI Add-on Board

For Sparrowhawk FX dev. board

USER'S MANUAL

UM0012

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Revision History

Revision	Date	Author	Modification
1.0	02.09.2014.	AS	Initial
1.1	07.09.2015	IP	Revamp

Related Documents

ID	Code	Description
1	UM0011	Sparrowhawk FX User's Manual

1 Introduction

Sparrowhawk FX Video Processing Board includes an expansion connection to support applications that can be implemented using SERDES. This expansion connection includes 8 additional SERDES input and output differential pairs of two whole SERDES quads available for expansion as SDI, or other video interfaces, the control/status signals, audio channels over IO pins and the power/ground pins.

The SDI Add-on board is a Sparrowhawk FX video processing board daughter card designed to support Serial Digital Interface (SDI) family of video interfaces standard from the Society of Motion Picture and Television Engineers (SMPTE) that transmits digital video data and embedded audio data through the 75-ohm coaxial cable.

SDI Add-on board includes:

- four SDI input channels,
- four SDI output channels,
- AES3 audio input,
- AES3 audio output,
- Genlock input,
- I2S Audio input,
- I2S Audio output.

The SDI input and output channels are mapped to two Lattice ECP3 SERDES quads through an expansion connector.

1.1 Application

- Frame grabbers
- DVRs
- Transcoding systems
- Professional video
- Surveillance
- Industrial video systems
- Machine vision
- Broadcast equipment

2 Board Features

Table 1: SDI Add-on board feature list

Category	Features
Video Interfaces	• **4x** SDI Input (BNC connector), SDI Equalizer (LMH0384) • **4x** SDI Output (BNC connector) , SDI Cable Driver (LMH0302)
Audio Interfaces	• TLV320AIC3007 stereo audio codec • Stereo Line Out • Stereo Line In • DIX4192 digital audio interface receiver and transmitter
Communication Interfaces	• I2C Bus

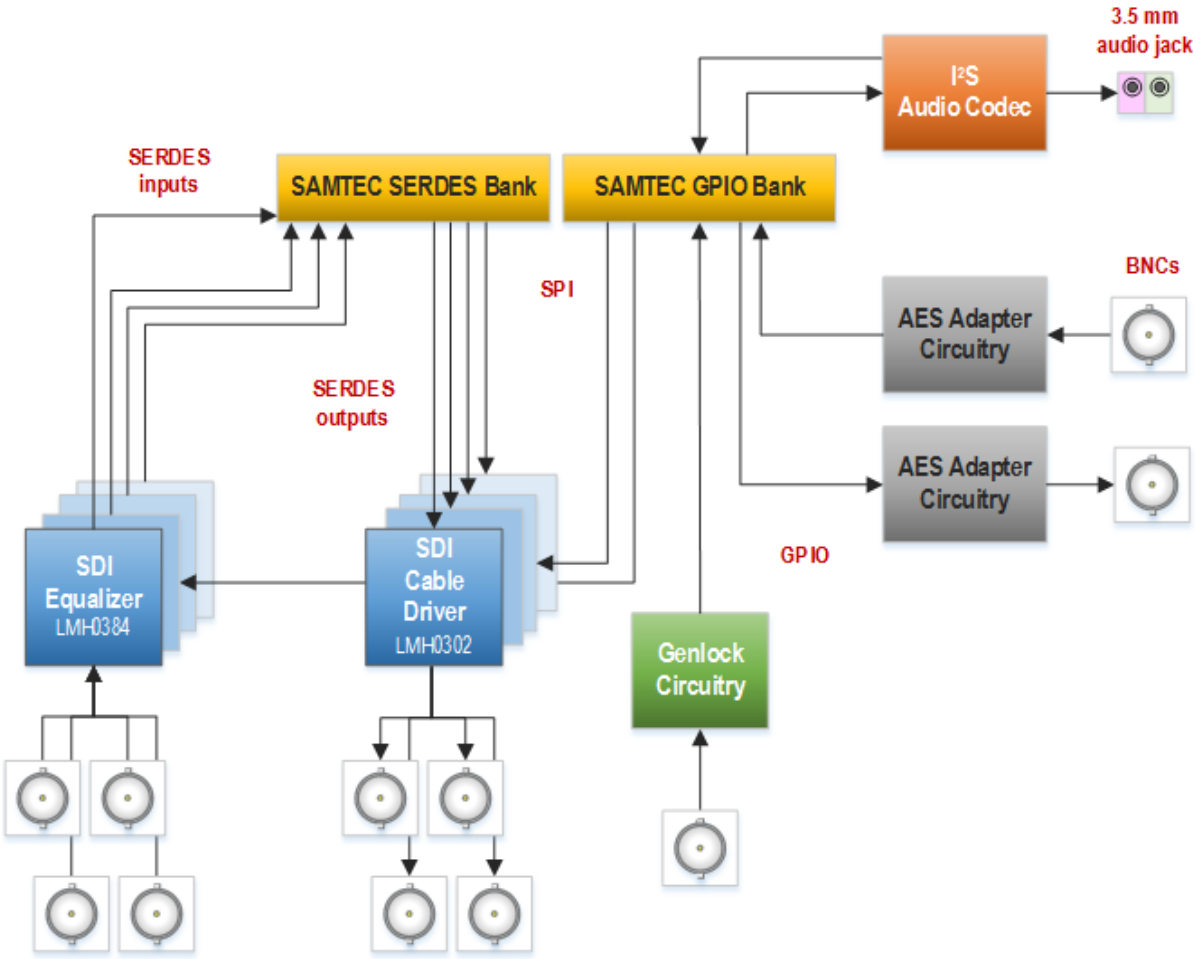
Board to board Interface ports	• Samtec QTH-060 Header Connector
	  ○ ***48x*** *GPIOs,*
	  ○ ***8x*** *SERDES In,*
	  ○ ***8x*** *SERDES Out,*
	  ○ ***1x*** *dedicated clock input*

Other peripherals	• **4x** Input video signal LED indication

Power Supply	• Interface header connector dedicated power pins (5V and 3V3)
	• Onboard linear voltage regulator
	  ○ *1V8*
	  ○ *2V5*

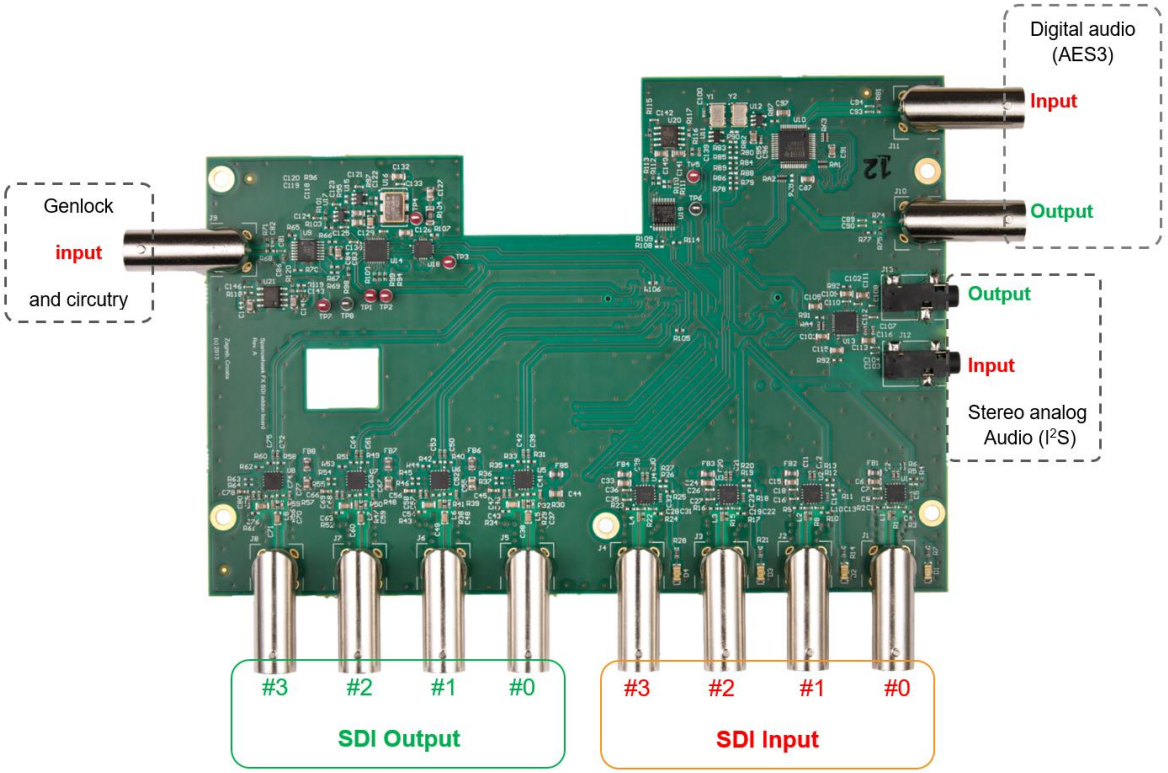
Video clocking	• Onboard Voltage Controlled oscillator • Genlock Circuitry (LMH1981 & LMH1982)
Manufacturing	• RoHS Compliant

2.1 Block Schematic



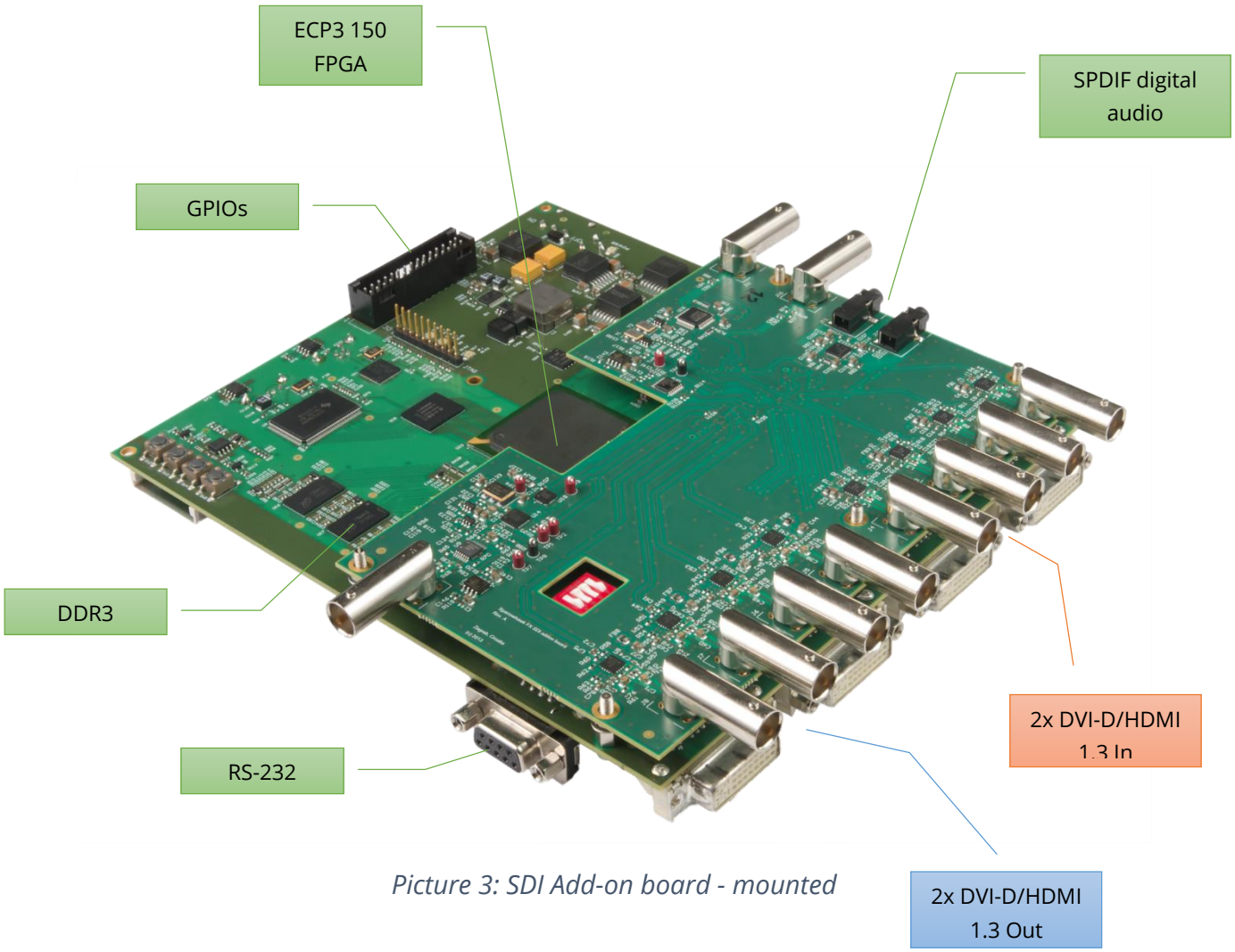
Picture 1: SDI Add-on board block diagram

2.2 Board Layout



Picture 2: SDI Add-on board layout – top

Picture 3 shows the SDI Add-on board installed on the Sparrowhawk FX video processing board.



Picture 3: SDI Add-on board - mounted

3 Powering up the board

CAUTION!

The SDI Add-on PCB is protected against ESD (Electro Static Discharge), but improper handling can still damage the board. Try to avoid touching non-insulated parts of the board. If possible, use a functioning ground strap whenever handling the board.

To power up the SDI Add-on board, it is necessary to plug it into the Sparrowhawk FX board (see picture 3). The SDI Add-on board is powered through the interface header connector dedicated power pins, providing 3.3 V and 5V to the board. Two instances of the Texas Instruments LP38511 low-dropout linear voltage regulator are used for providing the 1.8 V and 2.5 V to the board.

4 PCB details

The SDI Add-on board uses BNC connectors and equalizer ICs required for 4x SDI inputs and outputs. The SDI channels are connected to the FPGA through the Samtec QTH-060 header connector (Exp. Conn. #0 on the Sparrowhawk FX).

The PCB is designed to account to rigorous requirements of Tri-Rate SDI channels.

4.1 SDI video input

SDI video input is available via 4 BNC 75 Ohm connectors, J1, J2, J3 and J4. The SDI inputs are bridged between the BNC connectors and Lattice ECP3 150 FPGA on Sparrowhawk FX board through the TI LMH0384 cable equalizers. The connection to the FPGA is achieved by using fast differential pairs on the header connector J14 on the Add-on board (expansion connector J12 on the SHFX board).

The SDI input channels are mapped to Lattice ECP3 SERDES quads A and C.

SDI input channels of the connectors J1 and J2 are connected to the SERDES channels with associated quad C PCS logic, using 2 data channels and a dedicated clock input. SDI input channels of the connectors J3 and J4 are connected to the

SERDES channels with associated quad A PCS logic, using 2 data channels and a dedicated clock input.

SERDES de-serializes data into 20-bit words, which are processed into standard video signals by the Lattice Tri-Rate SDI PHY IP core.

The table below describes mapping between SERDES and BNC connectors /cable equalizers, and SERDES channel mapping inside each quad.

Table 2: SDI input SERDES mapping

BNC connector	Quad	Serdes RX channel
J1	PCSC	Channel #1
J2		Channel #2
J3	PCSA	Channel #1
J4		Channel #2

4.2 SDI video output

SDI video output is available via 4 BNC 75 Ohm connectors, J5, J6, J7 and J8. The SDI video output connectors are connected to Lattice ECP3 SERDES through TI LMH0302 SDI cable driver and fast differential pairs on the header connector J14.

The SDI output interfaces are mapped to Lattice ECP3 SERDES quads A and C.

SERDES can output fast differential signals required by the TMDS signaling. 10-bit words are serialized and transmitted using 3 output data channels, while the clock is outputted using the fourth output data channel.

Output channels of SERDES in FPGA are used for driving fast differential pairs for DVI output. The table below describes mapping between SERDES and DVI connectors, and SERDES channel mapping inside each connector.

Table 3: SDI output SERDES mapping

BNC connector	Quad	Serdes TX channel
J5	PCSC	Channel #1
J6		Channel #2
J7	PCSA	Channel #1
J8		Channel #2

4.3 Genlock

Genlock interface is used as a separate sync input to to the SDI processor. It allows precise synchronization of outputs to a standard time signal. Texas instruments LMH1981 and LMH1982 ICs are used for genlocking.

The LMH1981 is a high performance multi-format sync separator. The input automatically detects the input video format and accepts standard analog SD/ED/HD video signal with either bi-level or tri-level sync. The outputs provide composite, horizontal and vertical sync timing signals.

The LMH1982 is a multi-rate video clock generator that can generate two simultaneous low-jitter SD and HD clocks with selectable frequencies. In genlock mode, the device's phase locked loops can synchronize the output signals to one of the two available input reference ports with hsync and vsync signals. The input references connected to the LMH1982 on the SDI Add-on PCB are TI LMH1981 outputs on port A inputs, and timing signals from header connector J14 (ECP3 150 FPGA outputs from an SDI deserializer) to the port B inputs.

4.4 AES3

Digital audio IO is supported on the SDI Add-on by the Texas Instruments DIX4192 digital audio interface receiver and transmitter. The device supports four differential line input receivers, one differential line driver and two audio serial ports connected to ECP3 FPGA through interface header connector.

The board provides 1x AES3 stereo input and 1x AES3 stereo output with AES-3id interface which uses the same BNC connector as SDI and is used in broadcast applications.

The list of AES3 audio connectors is available in the table below.

Table 4: AES3 audio connectors

Audio conn	Conn type	Function	DIX4192 pin	
J10	Tx	Audio line-out	Tx+	32
			Tx-	31
J11	Rx	Audio line-in	Rx+	1
			Rx-	2

Table 5: DIX4192 interface pinout

DIX4192 pin	Signal
37	aes_bcka
38	aes_lrcka
39	aes_sdina
40	aes_sdouta
45	aes_bckb
46	aes_lrckb
47	aes_sdinb
48	aes_sdoutb
36	aes_sync
35	aes_bls
11	aes_lock
12	aes_rxcko
29	aes_gpo4
28	aes_gpo3
27	aes_gpo2
26	aes_gpo1
23	aes_intn
19	aes_cs
25	aes_mclk

4.5 I²S

I2S codec is supported on the SDI Add-on board by the Texas Instruments TLV320AIC3007 low power stereo audio codec IC.

There are two analog audio interfaces on board, stereo input and output via 3.5 mm jack connectors J12 and J13.

Table 6: AES3 audio connectors

Audio conn	Conn type	Function	TLV320AIC pin	
J12	Rx	Stereo line-in	LINE1LP	4
			LINE1RP	5
J13	Tx	Stereo line-out	HPLOUT	14
			HPCOM	15
			HPROUT	17

4.6 Interface connector

Header connector marked J14 is the Samtec QTH-060 high-speed mezzanine connector. It mates with the QSH-060-01-L-D-A connector (expansion connector #0 on SHFX board, marked J12). This board to board interface connector is divided into 2 banks, one dedicated to the high-speed differential pairs, the other to the general purpose IO pins. Each bank also has power supply pins, one 3.3V and one 5V. 2 pins are dedicated to the system I2C bus.

The connector pinout and the corresponding PCB signal mapping is shown below.

Table 7: Interface connector Bank 0 pinout and PCB signal mapping

EXP Pin	Function	Signal	EXP pin	Function	FPGA pin
1	3V3		2	3V3	
3	3V3		4	3V3	
5	3V3		6	3V3	
7	SDA	sys_sda	8	SCL	sys_scl
9	GPIO0	aes_sdoutb	10	GPIO1	i2s_bclk
11	GPIO2	aes_sdinb	12	GPIO3	i2s_wclk
13	GPIO4	aes_lrckb	14	GPIO5	i2s_din
15	GPIO6	aes_bckb	16	GPIO7	i2s_dout
17	GPIO8	aes_sdouta	18	GPIO9	i2s_mclk
19	GPIO10	aes_sdina	20	GPIO11	i2s_gpio1
21	GPIO12	aes_lrcka	22	GND	
23	GPIO14	aes_bcka	24	EXP_PLL_P	-
25	GPIO16	aes_sync	26	EXP_PLL_N	no_lock
27	GPIO18	aes_bls	28	GND	
29	GPIO20	aes_lock	30	GPIO13	spi_s_cs0_n
31	GPIO22	aes_rxcko	32	GPIO15	spi_s_cs1_n
33	GPIO24	aes_gpo4	34	GPIO17	spi_s_cs2_n
35	GPIO26	aes_gpo3	36	GPIO19	spi_s_cs3_n
37	GPIO28	aes_gpo2	38	GPIO21	spi_s_mosi
39	GPIO30	aes_gpo1	40	GPIO23	spi_s_clk
41	GPIO32	aes_intn	42	GPIO25	spi_s_miso
43	GPIO33	aes_cs	44	GPIO27	clk_sel0
45	GPIO34	aes_mclk	46	RFU	i2c_int
47	GPIO35	tof	48	GPIO31	clk_sel1
49	GPIO36	fpga_vsync	50	GPIO37	sdi_en_out0
51	GPIO38	fpga_hsync	52	GPIO39	sdi_en_out1
53	GPIO40	gl_oeout	54	GPIO41	sdi_sdhd_out0_1
55	GPIO42	gl_hsout	56	GPIO43	sdi_en_out2
57	GPIO44	gl_vsout	58	GPIO45	sdi_sdhd_out2_3
59	GPIO46	gl_vfout	60	GPIO47	sdi_en_out3

Table 8: Interface connector Bank 1 pinout and PCB signal mapping

EXP Pin	Function	Signal	EXP pin	Function	Signal
61	SERDES		**62**	SERDES	SDI_CLK_0_N
63	SERDES		**64**	SERDES	SDI_CLK_0_P
65	GND		**66**	GND	
67	SERDES	SDI_FPGA_OUT0_P	**68**	SERDES	
69	SERDES	SDI_FPGA_OUT0_N	**70**	SERDES	
71	GND		**72**	GND	
73	SERDES	SDI_FPGA_OUT1_P	**74**	SERDES	SDI_IN0_AC_N
75	SERDES	SDI_FPGA_OUT1_N	**76**	SERDES	SDI_IN0_AC_P
77	GND		**78**	GND	
79	SERDES		**80**	SERDES	SDI_IN1_AC_N
81	SERDES		**82**	SERDES	SDI_IN1_AC_p
83	GND		**84**	GND	
85	SERDES	SDI_CLK_1_N	**86**	SERDES	
87	SERDES	SDI_CLK_1_P	**88**	SERDES	
89	GND		**90**	GND	
91	SERDES		**92**	SERDES	
93	SERDES		**94**	SERDES	
95	GND		**96**	GND	
97	SERDES	SDI_FPGA_OUT2_P	**98**	SERDES	SDI_IN2_AC_N
99	SERDES	SDI_FPGA_OUT2_N	**100**	SERDES	SDI_IN2_AC_P
101	GND		**102**	GND	
103	SERDES	SDI_FPGA_OUT3_P	**104**	SERDES	SDI_IN3_AC_N
105	SERDES	SDI_FPGA_OUT3_N	**106**	SERDES	SDI_IN3_AC_P
107	GND		**108**	GND	
109	SERDES		**110**	SERDES	
111	SERDES		**112**	SERDES	
113	GND		**114**	GND	
115	5V		**116**	5V	
117	5V		**118**	5V	
119	5V		**120**	5V	

4.7 Test points

The board includes the following test points:

- TI Equalizer and driver reference design test points
  - Should allow duplication of tests from the TI reference board
  - SPI communication is a must
- All power voltage and GND test points
- GND scope clamp (as PCB edge or holes)
- I2S Interface
- AES3 interface
  - Inputs (from BNC)
  - Output to FPGA
- Genlock interface
  - Input from BNC
  - Output to FPGA

Table 9: SDI Add-on board test points

Test point	Description	Signal	Connection
TP1	Genlock interface vertical sync output	GL_VSOUT	LMH1981 pin 8
TP2	Genlock interface horizontal sync output	GL_HSOUT	LMH1981 pin 7
TP3		TOF	LMH1982 pin 25
TP4		VCXO	LMH1982 pin 29
TP5	1.8V power voltage	VCC_1V8	
TP6	ground	GND	
TP7	2.5V power voltage	VCC_2V5	
TP8	ground	GND	

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