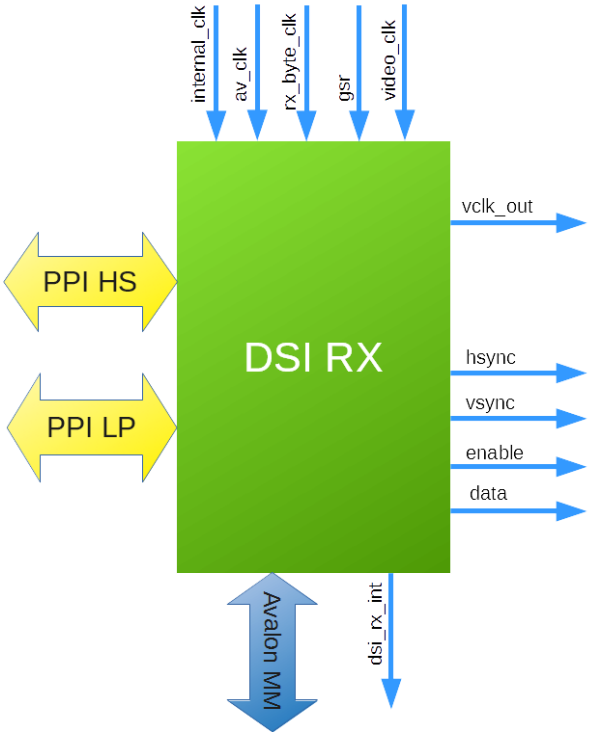
IQ-DSI-Rx

MIPI(r) DSI Receiver IP Core



Core Facts	
Core specifics	
Supported Device Family	MAX 10
Supported User Interfaces	PPI, AVALON MM, Display
Provided with Core	
Documentation	User's Manual
Design Files	VHDL
Example design	VHDL
Test bench	VHDL
Constraints File	Timing
Simulation tool used	
Modelsim Intel FPGA Edition	
Support	
Support Provided by Mikroprojekt d.o.o	

IQ-DSI-Rx is a MIPI DSI protocol engine/ receiver IP core designed to work with PPI-compatible MIPI D-PHY serial interfaces for driving embedded displays.

Features

- Programmable number of serial data lanes (1-4)
- Data rate from 80 to 800 Mbps per lane
- PHY-Protocol Interface (PPI) towards D-PHY
- Clocked video interface at output
- HS (High Speed) mode receiving support
- Supports all 24-bit, 18-bit and 16-bit DSI compatible video formats (rgb888, rgb565, YcbCr, ...),
- Video modes support (Non-burst with sync pulses, Non-burst with sync events)
- ECC checking for header
- CRC checking for packet payload
- Avalon-MM interface for register access
- Compliant to MIPI Alliance Specification for Display Serial Interface v1.3.1

Unsupported Features

- DSI Video command mode
- DSI Virtual channels
- LP data transfers and BTA

Core utilization

DEVICE	LE	REG	M9K	I/O
MAX 10	3187	1406	5	-

Ordering information

Please contact us via email **contact@mikroprojekt.hr** about item availability and ordering details.