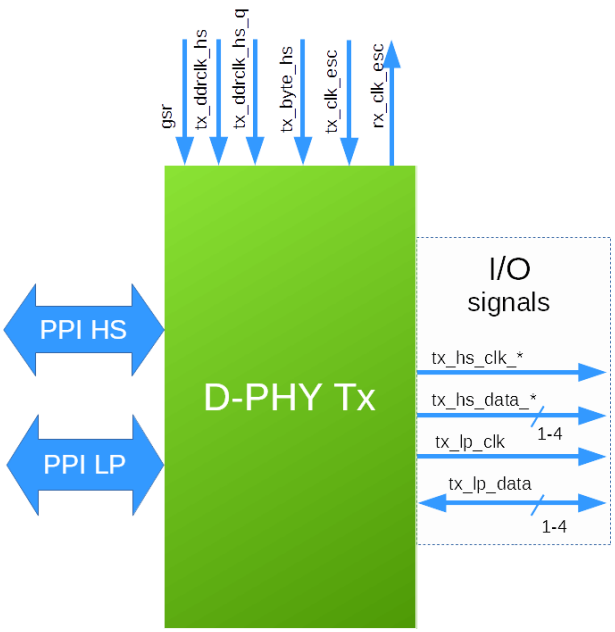
IQ-DPHY-Tx

PPI-Compatible MIPI(r) D-PHY Transmitter IP Core



Core Facts	
Core specifics	
Supported Device Family	MAX 10
Supported User Interfaces	PPI, Passive D-Phy
Provided with Core	
Documentation	User's Manual
Design Files	VHDL, Encrypted VHDL
Example design	VHDL
Test bench	VHDL
Constraints File	Timing
Simulation tool used	
Modelsim Intel FPGA edition	
Support	
Support Provided by Mikroprojekt d.o.o	

IQ-DPHY-Tx is a MIPI D-Phy transmit physical layer IP core for Intel FPGA devices. It is designed to work with protocol engines utilizing the PPI interface for accessing the MIPI D-PHY Bus.

Features

- One clock lane and up to four data lanes
- Unidirectional High speed mode with data rate up to 900 Mbps
- Bidirectional low power operation modes with data rate of 10 Mbps
- Ultra low power mode (ULPS) and high speed mode for clock lane
- Ultra low power mode, high speed mode and escape mode support for data lanes
- PHY-Protocol Interface (PPI) for connection to DSI and CSI-2 protocol layers
- Compliant to MIPI Alliance Specification for D-PHY v1.0.0

Unsupported Features

- Contention detection
- 8b9b Encoding

Core utilization (4 lanes)

DEVICE	LE	REG	M9K	I/O
MAX 10	667	565	0	20

Ordering information

Please contact us via email **contact@mikroprojekt.hr** about item availability and ordering details.