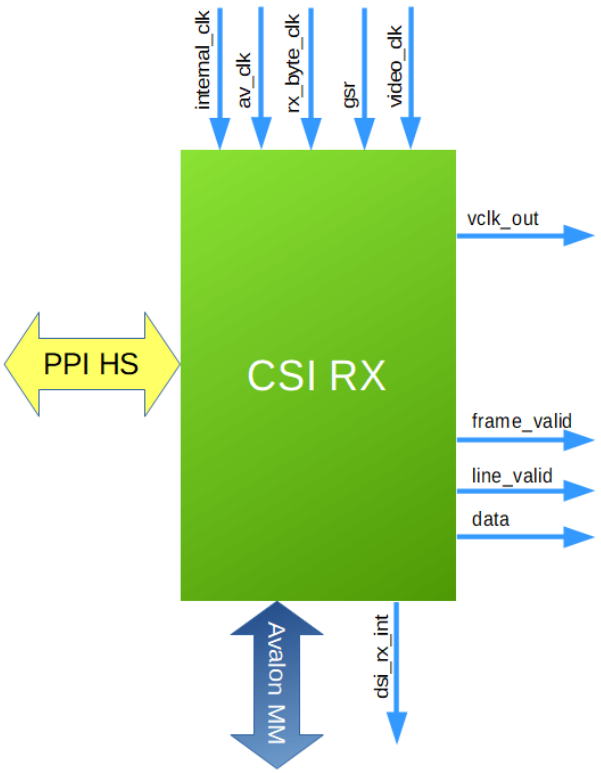
IQ-CSI-Rx

MIPI(r) CSI Receiver IP Core



Core Facts	
Core specifics	
Supported Device Family	MAX 10
Supported User Interfaces	PPI, AVALON MM, Display
Provided with Core	
Documentation	User's Manual
Design Files	VHDL
Example design	VHDL
Test bench	VHDL
Constraints File	Timing
Simulation tool used	
Modelsim Intel FPGA Edition	
Support	
Support Provided by Mikroprojekt d.o.o	

IQ-CSI-Rx is a MIPI CSI-2 protocol engine/ receiver IP core designed to work with PPI-compatible MIPI D-PHY serial interfaces for capturing images from MIPI CSI-2 camera sensors.

Features

- Programmable number of serial data lanes (1-4)
- Data rate from 80 to 800 Mbps per lane
- PHY-Protocol Interface (PPI) towards D-PHY
- Clocked video interface at output
- HS (High Speed) mode receiving support
- Supports all primary data formats (RAW, YUV, RGB...)
- ECC checking for header
- CRC checking for packet payload
- Avalon-MM interface for register access
- Compliant to MIPI Alliance Specification for Camera Serial Interface v1.3.1

Unsupported Features

- Virtual channels
- Secondary data types (RAW12 excluded)
- Data type interleaving

Core utilization

DEVICE	LE	REG	M9K	I/O
MAX 10	794	603	11	N/A

Ordering information

Please contact us via email **contact@mikroprojekt.hr** about item availability and ordering details.