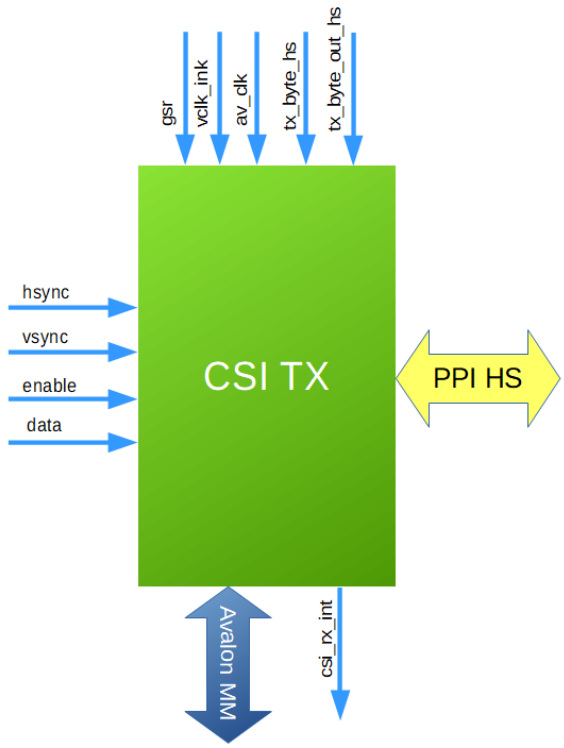
IQ-CSI-Tx

MIPI(r) CSI Transmitter IP Core



Core Facts	
Core specifics	
Supported Device Family	MAX 10
Supported User Interfaces	PPI, AVALON MM
Provided with Core	
Documentation	User's Manual
Design Files	VHDL
Example design	VHDL
Test bench	VHDL
Constraints File	Timing
Simulation tool used	
Modelsim Intel FPGA edition	
Support	
Support Provided by Mikroprojekt d.o.o	

IQ-CSI-Tx is a MIPI CSI-2 protocol engine/ transmitter IP core designed to work with PPI-compatible MIPI D-PHY serial interfaces for driving MIPI based image sensor processors.

Features

- Programmable number of serial data lanes (1-4)
- Data rate from 80 to 900 Mbps per lane
- PHY-Protocol Interface (PPI) towards D-PHY
- Clocked video interface at input
- HS (High Speed) mode transmission support
- LP (Low power) insertion between the packets
- Supports all primary video data formats (RAW, YUV, RGB)
- ECC generation for packet header
- CRC generation for packet payload
- Avalon-MM interface for register access
- Compliant to MIPI Alliance Specification for Camera Serial Interface v1.3

Unsupported Features

- Secondary data types
- Virtual channels
- Non-continuous clock mode

Core utilization

DEVICE	LE	REG	M9K	I/O
MAX 10	1179	889	10	N/A

Ordering information

Please contact us via email **contact@mikroprojekt.hr** about item availability and ordering details.