mikroprojekt

Sparrowhawk FX

Sparrowhawk FX development board

USER'S MANUAL

UM0011

Rev. 1.2

6.7.2016.

Table of contents

Revision History

Revision	Date	Author	Modification
0.1	06.09.2011.	SO	Initial
0.2	29.09.2011.	MR	Added board image and layout. Detailed some documentation. Added table captions. Added indexes of tables and figures. Better outline of expansion connectors.
1.0	16.07.2015.	MR	Updated to board rev. B details. General information update
1.1	09.12.2015.	IP	Revamp – New Template
1.2	06.07.2016.	IP	New board layouts (pictures & annotations)

Related Documents

ID	Code	Description

1 Introduction

The Sparrowhawk FX is an FPGA development board targeted for video acquisition, processing, and display applications, based on the award-winning Lattice ECP3 FPGA.

The Sparrowhawk FX board implements Mikroprojekt's IQ-Video solution, powered by the Peregrine system interconnect and Mikroprojekt's IP cores, enabling high performance computation. In conjuction with fast DDR3 Memory, the Sparrowhawk FX allows for reception, processing, arbitrary mixing and display of 4 independent DVI/HDMI video input and output streams in full HD 1080p60 resolution (1920x1080 @ 60 Hz, 24-bit color), with room to handle also the emerging 4k*2k video for next generation digital cinemas.

The IQ-Video solution employs Mikroprojekt's IP cores for video reception, display driving, and memory control to receive high definition video from the external interfaces. The IQ-ScalR IP core allows for high quality, gradual scaling effects on video reception, after which the image is received and recorded to the memory by the IQ-VIN frame grabber. The IQ-DispML Multilayer Display Controller allows the display and compositing of multiple video streams and graphics by means of alpha blending, enabling Picture-in-Picture (PIP) and On-Screen Display (OSD) functionalities.

Reception and transmission of HDMI video streams is performed by Mikroprojekt's IQ-HDMI-Rx and IQ-HDMI-Tx IP cores, serving as DVI/HDMI video decoders and encoders, able to receive and transmit both video data and HDMI info frames, enabling the Sparrowhawk Fx to transmit, receive and process HDMI audio data. Sound input and playback is also supported through an onboard AC'97 audio codec.

While two inputs and two outputs are implemented on the board as DVI/HDMI, the remaining 2 SERDES I/O quads are connected to expansion ports. This allows the board to be expanded not only with the DVI/HDMI, but also with SDI and HD-SDI, DisplayPort, V-by-One HS, or other interfaces, such as Gigabit Ethernet.

The solution is controlled by the Lattice Mico32 Soft CPU implemented within the FPGA fabric. The Mico32 CPU allows precise control of the video timing, transition effects, and also supports the generation of OSD graphics within the solution, allowing the board to operate as a stand-alone video processor. Multiple Mico32 CPU cores can be added to control specific tasks. For high-quality OSD graphics generation, Mikroprojekt's IQ-GraphBlit 2D accelerator can be integrated.

Program data, graphics data and various parameters can be stored in the onboard parallel NOR flash device, or the SPI flash device used also for the FPGA design storage. An SD Card slot with a full SD card interface is also provided. Buttons, DIP switches and LEDs are provided for basic communication and control of the system.

A high speed USB interface/debug link is supported, as well as the USB host functionality, allowing the board to interface to USB touchscreens or Web cameras. A standard RS-232 port is also provided for debug and configuration purposes.

1.1 Applications

- Digital signage
  - Video walls
  - Visual installations
- 3D display systems
  - Stereoscopic displays
  - Projection systems
  - Autostereoscopic displays
- Video acquisition systems
- Real-time video processing and mixing
- Machine vision
- Real time video format conversion/transcoding
- Multiple display driving

2 Board Features

Table 1: Sparrowhawk FX feature list

Category	Features
FPGA	Lattice ECP3 LFE3-150EA-8FN1156 149.000 LUTs 372 Block RAMs 320 18x18 Multipliers 586 IO pins 16 SERDES channels (In/out) 400 MHz DDR3 Memory Support 10 PLLs, 2 DLLs
Video Memory	DDR3-800 (4) 4x Micron MT41J64M16JT-15E 400 MHz Clock Dual 32-bit channel (2x2 chips) 6.4 GB/s (theoretical maximum) 512 MB Total memory (expandable to 1024 MB)
Video interfaces	2x DVI/HDMI Input (DVI connector) 2x DVI/HDMI Output (DVI connector) DDC Supported on all in/out connectors
Nonvolatile storage	Numonyx M29EW Parallel NOR Flash 512Mbits (64MB) – expandable to 2Gbits (256 MB) ST M25P64 SPI Flash (Stores FPGA Configuration) Secure Digital Card slot
Audio Interfaces	Wolfson WM9707 AC'97 2.1 Audio Codec Stereo Line In & Out S/PDIF Out
Communication Interfaces	Cypress CY7C68013A USB 2.0 Device STEricsson ISP1760 USB 2.0 Host RS-232 Interface I2C Bus (On all expansion connectors)
Expansion ports	Expansion Connectors (3) • 1x Low Cost Expansion 2.54mm 30-pin header (22 GPIOs) • 1x Samtec QSH-060 Expansion Connector (48 GPIOs, 8 SERDES In, 8 SERDES Out, 1 dedicated clock input) • 1x Samtec QSH-030 Expansion Connector (44 GPIOs, 2 dedicated clock inputs) 114 GPIO pins in total
Other peripherals	Push-buttons (4) DIP Switches (4) LEDs (8)
Power Supply	12V DC Input Power switch Onboard 5V, 3V3, 1V2 Switching power supplies, Onboard 1V5 DDR3 Switching power supply, Onboard FPGA 1V2 Core voltage linear regulator
Clocking	Onboard 100MHz Oscillator Onboard Programmable Clock Generator for SERDES/Video Interfaces – SiLabs
Manufacturing	RoHS Compliant

2.1 Block schematic

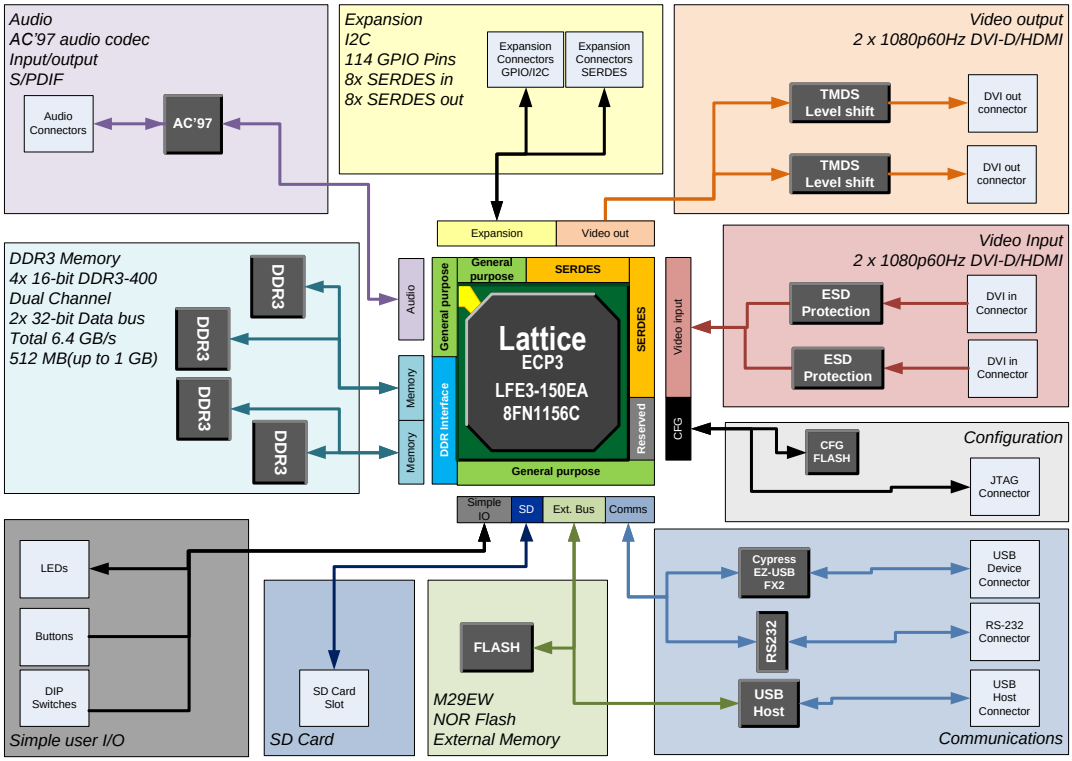


Figure 1: Sparrowhawk FX block diagram

2.2 Board layout

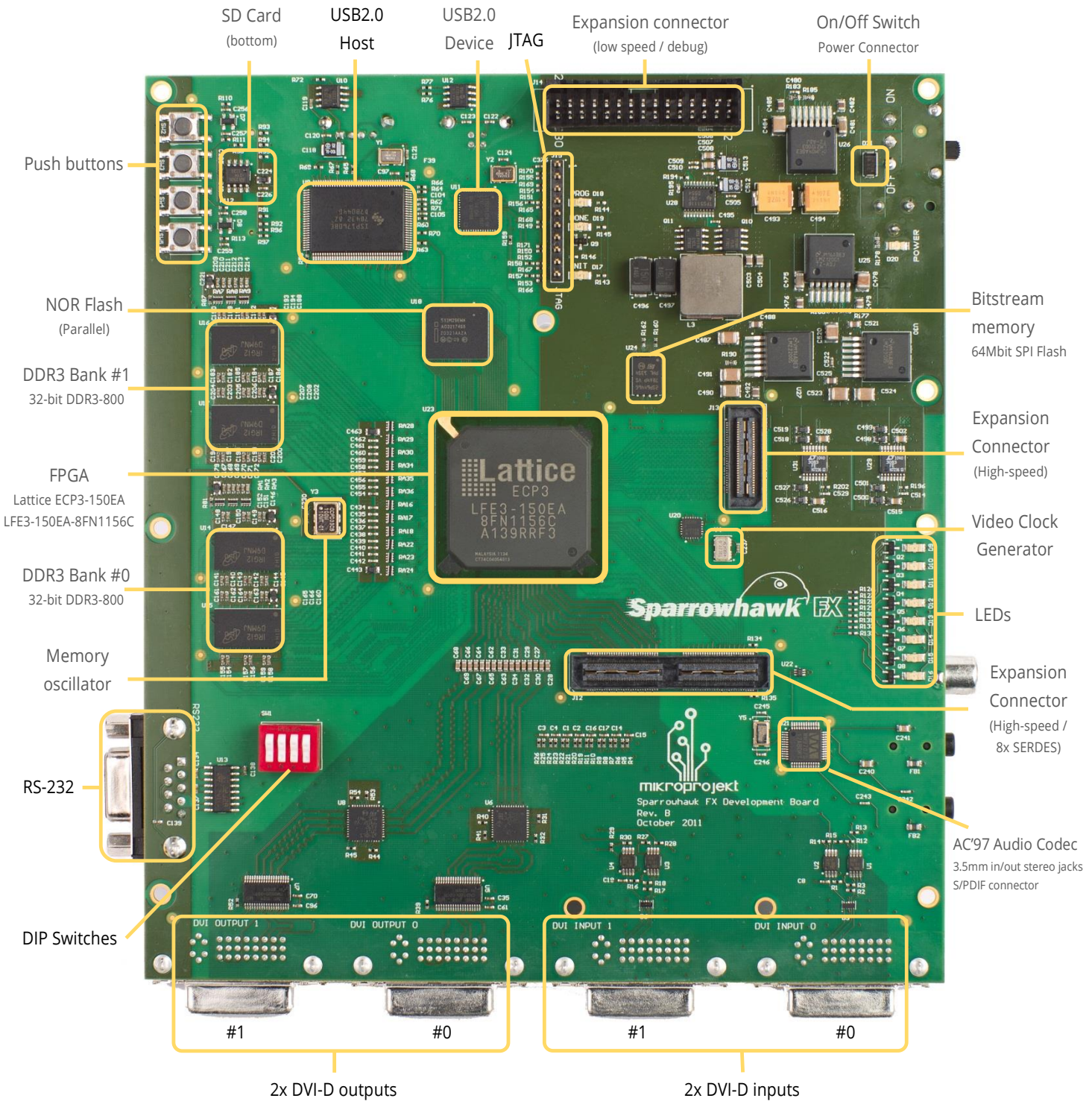


Figure 2: Sparrowhawk FX board layout – top

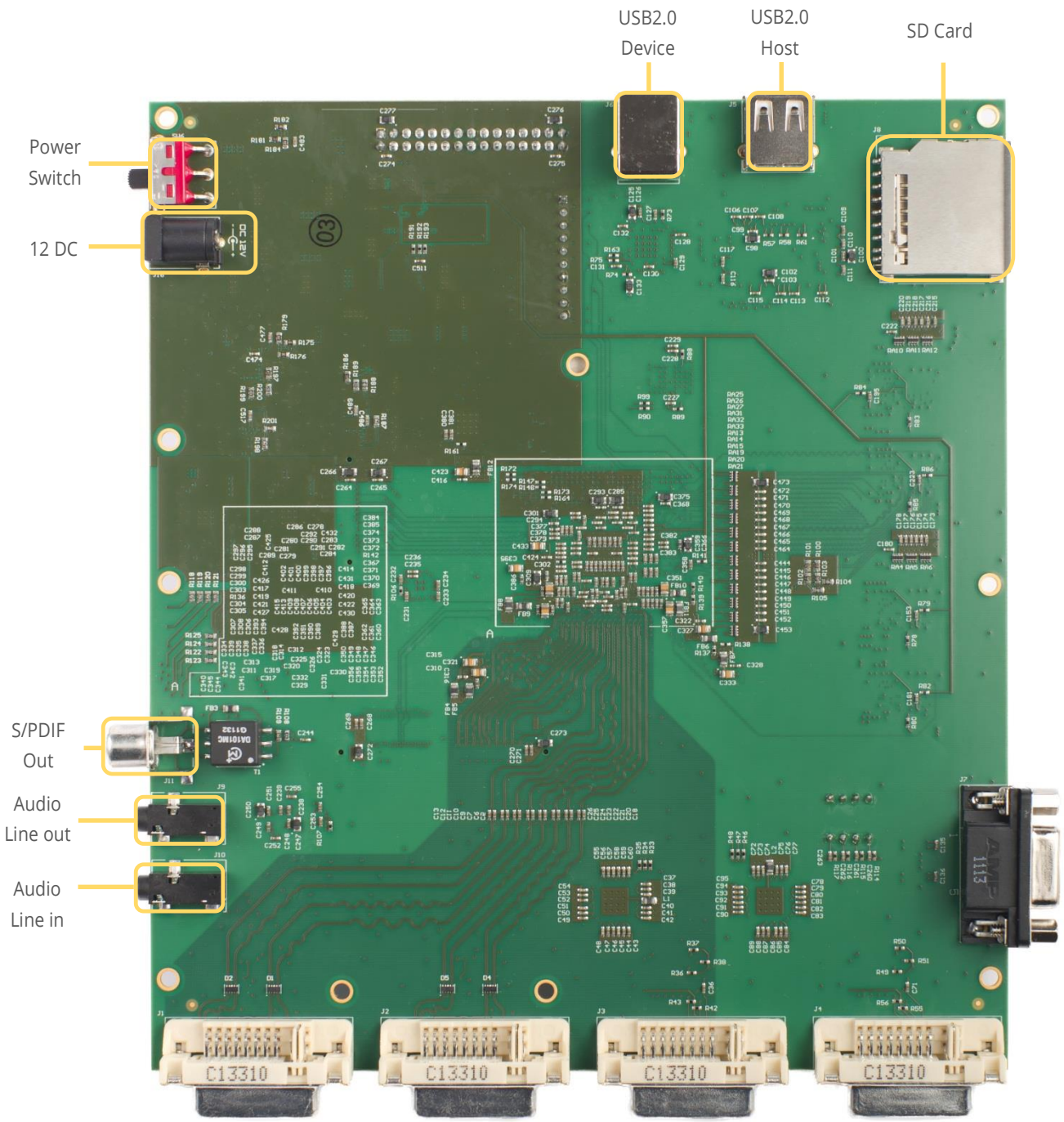


Figure 3: Sparrowhawk FX Board Layout – bottom

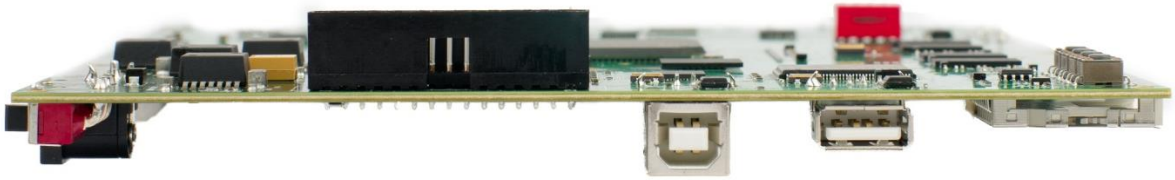


Figure 4: Sparrowhawk FX Board - top side view

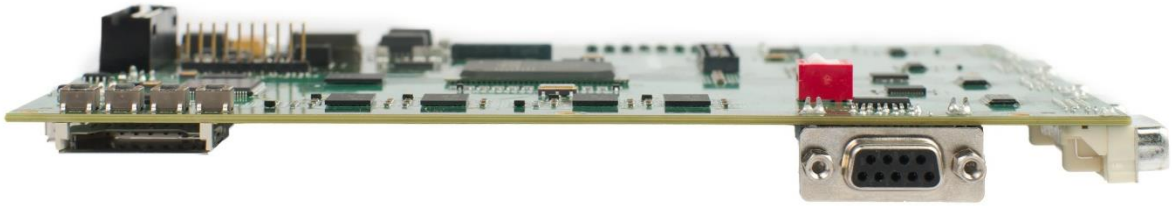


Figure 5: Sparrowhawk FX board - left side view

Figure 6: Sparrowhawk FX board - bottom side view

Figure 7: Sparrowhawk FX board – right side view

3 Powering up the board

CAUTION!

The Sparrowhawk FX PCB is protected against ESD (Electro Static Discharge), but improper handling can still damage the board. Try to avoid touching non-insulated parts of the board, especially DDR3 and the expansion connectors. If possible, use a functioning ground strap whenever handling the board.

The Sparrowhawk FX is delivered with the FPGA demo design in the SPI boot flash, and it will boot automatically after providing power and turning it on. The power can be supplied by the AC transformer provided with the board, or any type of DC supply source, providing 12V DC and a minimum of 18W.

The 12V DC power supply should be connected to the connector J16 on the bottom side of the board. The Sparrowhawk FX is protected by the diode D12 from the reverse power connection. The board is turned on/off by toggling the switch SW6, with "ON" and "OFF" marked in the silkscreen on the top of the board.

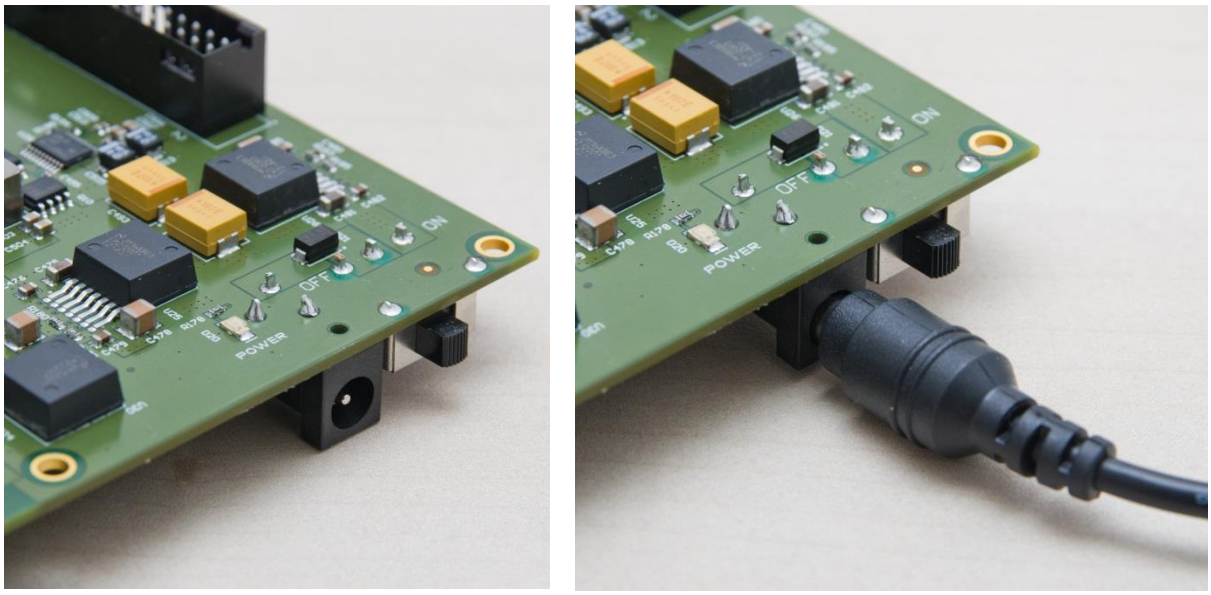


Figure 8: Sparrowhawk FX 12VDC Power Connection

3.1 FPGA configuration

3.1.1 JTAG

ECP3-150EA can be configured by ispVM download cable, connected to the JTAG header. 3 LEDs are provided for monitoring the download status, INIT, PROGRAM and DONE. ECP3 is the only device connected to the JTAG daisy chain. FPGA configuration can be downloaded to the M25P64 SPI Flash as well, using the ispVM programming cable. FPGA is configured to boot from the SPI Flash after power-up.

Table 2: JTAG Header pinout

JTAG header	Conn pin	Function
J15	1	3.3V Power
	2	TDO
	3	TDI
	4	PROGRAMN
	5	NC
	6	TMS
	7	GND
	8	TCK
	9	DONE
	10	INITN

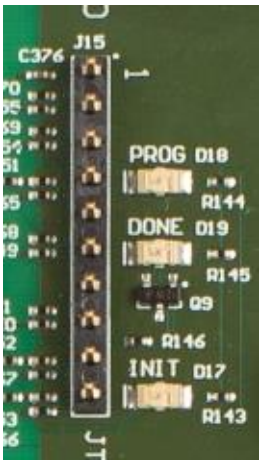


Table 3: JTAG LEDs

LED diode	Color	Function
D9	Red	INIT
D10	Red	PROGRAM
D11	Green	DONE

3.1.2 USB

Additionally, the SPI lines, FPGA reset and PROG lines, and the FPGA configuration control lines CFG2:0 can be controlled via the onboard Cypress EZ-USB FX2LP USB microcontroller. In this case, the bitstream can be programmed to the SPI flash, or downloaded to the FPGA in SPI Slave serial mode, from the host system over USB.

4 PCB details

The Sparrowhawk FX PCB was designed primarily as a high resolution video processing platform. To that end, the fastest devices on board are high-speed display links and DDR3 memory. Besides that, the Sparrowhawk FX features a wide range of support devices, enabling SW development, high-speed communication, data storage and a wide range of expansion.

4.1 Video input

Video input is available via 2 DVI connectors, J1 and J2. Further expansion is available by using fast differential pairs on expansion connector J12 and any of the standard IO pins available on the expansion connectors J12, J13 or J14 (i.e. by driving the signals directly, or through use of the external video decoders connected to the FPGA through the expansion connectors).

DVI input connectors are connected directly to the SERDES channels, using 3 data channels and a dedicated clock input. SERDES de-serializes data into 3x10-bit words, which are processed into standard video signals by the IQ-HDMI-Rx IP core. Besides TMDS signals, DDC and HPD signals are also routed to the FPGA, with level translation done in the ESD protection chips.

Table 4: DVI Input DDC pinout and FPGA mapping

DVI connector	DVI pin	FPGA pin	Bank
J1	HPD	W28	3
	DDC_SDA	V28	3
	DDC_SCL	V27	3
J2	HPD	V26	3
	DDC_SDA	W27	3
	DDC_SCL	W26	3

Input channels of SERDES in FPGA are used for receiving fast differential pairs from the DVI inputs. The table below describes mapping between SERDES and DVI connectors, and SERDES channel mapping inside each connector.

Table 5: DVI Input SERDES mapping

DVI connector	DVI video	SERDES	RX channel
J1	TMDS clock	PCSB	Clock input
	TMDS data 0		Channel #0
	TMDS data 1		Channel #1
	TMDS data 2		Channel #2
J2	TMDS clock	PCSD	Clock input
	TMDS data 0		Channel #0
	TMDS data 1		Channel #1
	TMDS data 2		Channel #2

4.2 Video output

Video output is available via 2 DVI connectors, J3 and J4. Further expansion is available by using fast differential pairs on expansion connector J12 and any of the standard IO pins available on the expansion connectors J12, J13 or J14 (i.e. by driving the signals directly or through use of the external video encoders connected to the FPGA through the expansion connectors).

SERDES can output fast differential signals required by the TMDS signaling. 10-bit words are serialized and transmitted using 3 output data channels, while the clock is outputted using the fourth output data channel. ECP3 cannot drive TMDS signals directly, so a signal conditioning chip STHDLS101T is added to the SERDES outputs dedicated to the DVI connector. This chip is controlled by the two enable pins, one for the TMDS outputs and one for the voltage level translators of the DDC and HPD pins. In addition to the SERDES lines, DDC lines (SDA and SCL) and the HPD line are connected through the STHDLS101T. They are also voltage-translated from 5V (DVI connector) to 3.3 V, because FPGA cannot receive or drive 5V. This is done by the ESD protection chip CM2020.

Table 6: DVI output DDC pinout and FPGA mapping

DVI connector	STHDLS101T port	FPGA pin	Bank
J3	OE_N	Y25	3
	DDC_EN	Y26	3
	HPD_SOURCE	AA28	3
	SDA_SOURCE	AA27	3
	SCL_SOURCE	AB27	3
J4	OE_N	AB26	3
	DDC_EN	AA26	3
	HPD_SOURCE	AB25	3
	SDA_SOURCE	AC25	3
	SCL_SOURCE	AA25	3

Output channels of SERDES in FPGA are used for driving fast differential pairs for DVI output. The table below describes mapping between SERDES and DVI connectors, and SERDES channel mapping inside each connector.

Table 7: DVI output SERDES mapping

DVI connector	DVI video	SERDES	TX channel
J3	TMDS clock	PCSB	Channel #3
	TMDS data 0		Channel #2
	TMDS data 1		Channel #1
	TMDS data 2		Channel #0
J4	TMDS clock	PCSD	Channel #3
	TMDS data 0		Channel #2
	TMDS data 1		Channel #1
	TMDS data 2		Channel #0

4.3 Clock generation

The Sparrowhawk FX has several clock oscillators and one programmable clock generator, intended for generation of the output video clock. The list of clock sources available to the FPGA devices is available below:

Table 8: Clock sources FPGA mapping

Clock source	Description	Clock	FPGA pin	FPGA function
Y3	100 MHz clock oscillator	CLK_100_P	U6	PLL
		CLK_100_N	U7	PLL
U18	Si5338 programmable clock generator	VID_CLK_0	U28	PCLK
		VID_CLK_1	Y28	PLL
U9	CY7C68013A clock output, with frequency programmable by SW.	CY_CLKOUT	P30	PLL

4.3.1 100 MHz clock oscillator

100 MHz clock oscillator is the primary clock source for the FPGA. It is connected to the DDR3 bank, for use with the DDR3 interface logic and as the main FPGA clock source.

4.3.2 Si5338 clock generator

Si5338 is a clock generator configurable by I2C bus (connected to the system I2C on the Sparrowhawk FX). A wide range of frequencies is available, with two separate outputs connected to the FPGA. The Si5338 is mapped to the I2C address 0x70.

4.3.3 CY7C68013A clock output

CY7C68013A microcontroller uses an external 24 MHz oscillator for internal clock generation. Depending on the SW settings, internal clock can be 12, 24 or 48 MHz, and this clock can be outputted for FPGA use (this has to be enabled by SW).

4.4 DDR3 memory

The Sparrowhawk FX PCB features 4 DDR3 modules Micron MT41J64M16, totaling 1024 MB of memory. The board can be expanded by mounting MT41J128M16, expanding the memory capacity to 2048 MB.

The memory is connected in the 2x2 configuration, enabling simultaneous use of 2 32-bit DDR3 data buses, both operating on 400 MHz clock frequency. Available bandwidth is therefore 6.4GB/s.

The memory is connected to the FPGA in banks 6 and 7. These are the only banks on the FPGA not operating on 3.3 V, they operate on the 1.5 V DDR3 power supply. They also use voltage reference of 0.75 V also provided by the DDR3 power supply, connected to the dedicated pins in the banks.

Table 9: Voltage references to be used as input

Vref pin	FPGA pin	Bank
VREF1_6	V7	6
VREF1_7	R9	7

These pins should never be used for IO, even when not using the DDR3 memory. If using only one of the banks, it is recommended to add dummy logic to the Vref pin in the unused bank, using Vref pin as input, and to set PULLMODE=NONE. Otherwise, FPGA design may place a weak pull-up on one of the Vref pins, forcing reference above 0.75V.

4.5 Audio

Audio IO is supported on the Sparrowhawk FX PCB by an AC'97 codec WM9707. The device supports analog line-in, analog line-out and digital output S/PDIF. The device is controlled from the FPGA by the standard serial AC'97 interface. The list of audio connectors is available in the table below.

Table 10: Audio connectors

Audio conn	Conn type	Function
J9	3.5mm audio	Audio line-out
J10	3.5mm audio	Audio line-in
J11	RCA	S/PDIF

Table 11: AC'97 interface pinout and FPGA mapping

AC'97 signal	FPGA pin	FPGA dir	Bank
RST_N	W29	out	3
CLK	V31	in	3
SDO	V29	out	3
SDI	V30	in	3
SYNC	W30	out	3

4.6 USB

The Sparrowhawk FX has USB device and USB host ports. The table below lists USB connectors on the PCB:

Table 12: USB connectors

USB conn	Conn type	Function
J5	USB A Receptable	USB host connector
J6	USB B Receptable	USB device connector

4.6.1 USB Host

The USB host connector is connected to the ISP1760 USB 2.0 host controller, providing FPGA control over myriad USB devices available today. ISP1760 is connected to the FPGA over the parallel bus, shared with the M29EW flash. The RD_N, WR_N, A0-A15 and D0-D15 are shared with the corresponding flash signals. The independent signals are listed in the table below:

Table 13: USB Host

USB HOST signal	FPGA pin	FPGA dir	Bank
RST_N	A16	Out	0
CS_N	B16	Out	0
INT	D17	In	0
DREQ	C16	Out	0
DACK	C17	In	0

4.6.2 USB Device

The USB device connector is connected to the Cypress CY7C68013A, USB 2.0 device controller providing up to 30MB/s throughput. CY7C68013A is connected to the FPGA through a FIFO interface, enabling high-speed data flow between USB host (i.e. PC) and FPGA.

Table 14: USB Device Slave FIFO pinout and FPGA mapping

USB Dev. Signal	FPGA pin	FPGA dir	Bank	USB Dev. Signal	FPGA pin	FPGA dir	Bank
IFCLK	E19	In	1	PB0	B17	inout	1
SLRD	A22	out	1	PB1	A17	inout	1
SLWR	B22	out	1	PB2	B18	inout	1
SLOE	D22	out	1	PB3	A18	inout	1
ADR0	C22	out	1	PB4	D19	inout	1
ADR1	B21	out	1	PB5	C19	inout	1
PKTEND	A21	out	1	PB6	B19	inout	1
FLAGA	C20	in	1	PB7	A19	inout	1
FLAGB	B20	in	1	INT0	E21	out	1
FLAGC	A20	in	1	INT1	D21	out	1

4.7 RS-232

One RS-232 interface is included on the Sparrowhawk FX board, connected over the voltage translator ST3232 to the female DB-9 connector. The pinout of the RS-232 connector is provided in the table below:

Table 15: RS-232 pinout and FPGA mapping

UART signal	UART pin	FPGA pin	FPGA dir	Bank
RX	2	C2	Out	0
TX	3	D4	In	0
RTS	7	C3	In	0
CTS	8	D3	Out	0

4.8 I2C

A system-wide I2C bus is used for configuration of the Si5338 clock generator, and it is also connected to the dedicated pins on both Samtec expansion connectors (J12 and J13). Si5338 has a fixed 7-bit I2C address 0x70, that is an 8-bit address 0xE0 for write and 0xE1 for read, so no devices with these addresses should be connected to the system I2C (i.e. mounted to the expansion connectors).

Table 16: System I2C pinout and FPGA mapping

I2C signal	FPGA pin	FPGA dir	Bank
SDA	AN32	inout	3
SCL	AN31	inout	3

A separate I2C bus is used by the Cypress CY7C68013A for access to the I2C EEPROM, containing VID and PID and possibly execution code for the 8051. EEPROM is on a fixed 7-bit I2C address 0x51, that is an 8-bit address 0xA2 for write and 0xA3 for read. This bus is also connected to the FPGA, for monitoring and direct access by the Mico32.

Table 17: Cypress I2C Pinout and FPGA Mapping

I2C signal	FPGA pin	FPGA dir	Bank
SDA	E18	inout	1
SCL	D18	inout	1

4.9 LEDs and switches

The system integrates 8 status LEDs, 4 DIP-style switches and 4 push buttons. LEDs are stacked in two rows, D1 – D4 and D5 – D8.

Table 18: LED pinout and FPGA mapping

LED diode	Color	FPGA pin	FPGA dir	Bank
D1	Green	G23	out	1
D2	Yellow	H23	out	1
D3	Red	H22	out	1
D4	Blue	G21	out	1
D5	Green	G26	out	1
D6	Yellow	H26	out	1
D7	Red	G25	out	1
D8	Blue	H25	out	1

DIP switches are connected to a pull-down RC network, when a switch is open, FPGA has '0' on the respective input, when a switch is closed FPGA has '1' on the respective input.

Table 19: DIP Switch pinout and FPGA mapping

DIP	FPGA pin	FPGA dir	Bank
DIP #0	A33	in	8
DIP #1	A32	in	8
DIP #2	B32	in	8
DIP #3	C32	in	8

Push-button switches are connected to a pull-down RC network, when a switch is open, FPGA has '0' on the respective input, when a switch is closed FPGA has '1' on the respective input.

Table 20: Pushbutton pinout and FPGA mapping

Push-button	FPGA pin	FPGA dir	Bank
SW2	E11	in	0
SW3	E10	in	0
SW4	F10	in	0
SW5	F12	in	0

4.10 Non-volatile storage

Several nonvolatile storage devices are available on the Sparrowhawk FX PCB:

4.10.1 Numonyx Axcell M29EW NOR Flash

The board integrates a parallel asynchronous NOR flash for storage of bulk data with fast access, such as test images, splash screens, and microcontroller software. The internal flash controller supports fast page read mode to extract maximum reading performance, up to 30 MB/s. TrueFFS flash file system implementation is feasible on the device. The device is connected to the FPGA over the parallel bus shared with the ISP1760 USB host controller.

Table 21: NOR Flash pinout and FPGA mapping

Flash signal	FPGA pin	FPGA dir	Bank	Flash signal	FPGA pin	FPGA dir	Bank
A0*	C5	out	0	A1*	D15	out	0
A2*	D16	out	0	A3*	B15	out	0
A4*	A14	out	0	A5*	C14	out	0
A6*	E15	out	0	A7*	B14	out	0
A8*	B11	out	0	A9*	A11	out	0
A10*	D12	out	0	A11*	C11	out	0
A12*	B10	out	0	A13*	A10	out	0
A14*	A8	out	0	A15*	A7	out	0
A16	B7	out	0	A17	A13	out	0
A18	D14	out	0	A19	E12	out	0
A20	C13	out	0	A21	D13	out	0
A22	A9	out	0	A23	B8	out	0
A24	A6	out	0	A25**	B6	out	0
A26**	A15	out	0	BUSY_N	B13	In	0
RD_N*	C4	out	0	WR_N*	A12	out	0
RST_N	B12	out	0	CS_N	D5	out	0
D0*	C6	inout	0	D1*	B1	inout	0
D2*	D9	inout	0	D3*	A2	inout	0
D4*	A3	inout	0	D5*	C10	inout	0
D6*	B4	inout	0	D7*	D11	inout	0
D8*	D6	inout	0	D9*	B2	inout	0
D10*	C8	inout	0	D11*	B3	inout	0
D12*	C9	inout	0	D13*	A4	inout	0
D14*	D10	inout	0	D15*	A5	inout	0

* Indicates pin is shared with ISP1760

** Not used on mounted device

4.10.2 SD Card slot

Secure digital cards (SD/SDHC/SDXC) are supported on the Sparrowhawk FX board, and a slot is present on the board. SD cards support multi-gigabyte storage for embedded video and graphics.

As per the SD specification, the power to the SD card is controlled by the SW (i.e. FPGA), using a MIC2505 switch controlled by the SDC_PWR_N signal. Setting this signal to '0' enables power to the SD card, and setting it to '1' disables it.

Table 22: SD Card pinout and FPGA mapping

SD conn	SD signal	SD pin	FPGA pin	FPGA dir	Bank
J7	DAT3/CS_N	1	G13	inout	0
	CMD/DI	2	G12	inout	0
	VSS	3			
	VDD	4			
	CLK/SCK	5	G11	out	0
	VSS	6			
	DAT0/DO	7	H12	inout	0
	DAT1/IRQ	8	H11	inout	0
	DAT2/NC	9	F13	inout	0
	CD_N	CD	E13	in	0
	WP	WP	J12	in	0
	SDC_PWR_N		H13	out	0

4.10.3 SPI Flash

An ST M25P64 SPI flash is connected to the FPGA. This device serves as the FPGA design storage, and can be accessed for field updates of the board's FPGA over software. Additionally it can hold an additional "safe" FPGA image for dual boot, software for an embedded microprocessor, or application-specific data.

Table 23: SPI flash pinout and FPGA mapping

SPI Flash	SPI signal	FPGA pin	FPGA dir	Bank
U22	CS_N	D34	out	8
	CLK	F34	out	8
	MOSI	F33	out	8
	MISO	F32	in	8

4.11 Expansion connectors

The board features several expansion connectors, 2 high-speed for high performance expansion PCBs and one low-speed for debug and slow IO expansion. All expansion connectors have dedicated power pins, providing 3.3 V and 5V to the expansion boards. High-speed connectors have dedicated system I2C pins as well.

4.11.1 EXP #0

Expansion connector #0 is the Samtec QSH-060-01-L-D-A high-speed mezzanine connector, marked J12. It mates with the QTH-060 connector, with the recommended mating height of 11mm or more (set by the choice of the QTH-060 connector). This expansion connector is divided into 2 banks, one dedicated to the high-speed differential pairs, the other to the general purpose IO pins. Each bank also has power supply pins, one 3.3V and one 5V. 2 pins are dedicated to the system I2C bus.

The connector pinout and the corresponding FPGA mapping is shown below.

Table 24: Expansion connector #0 Bank 0 pinout and FPGA mapping

EXP Pin	Function	FPGA pin	FPGA dir	Bank	EXP pin	Function	FPGA pin	FPGA dir	Bank
1	3V3				**2**	3V3			
3	3V3				**4**	3V3			
5	3V3				**6**	3V3			
7	SDA	AN32	inout	3	**8**	SCL	AN31	inout	3
9	GPIO0	W34	inout	3	**10**	GPIO1	AF32	inout	3
11	GPIO2	W33	inout	3	**12**	GPIO3	AF34	inout	
13	GPIO4	Y34	inout	3	**14**	GPIO5	AG34	inout	3
15	GPIO6	Y33	inout	3	**16**	GPIO7	AH33	inout	3
17	GPIO8	AB34	inout	3	**18**	GPIO9	AJ31	inout	3
19	GPIO10	AB33	inout	3	**20**	GPIO11	AJ33	inout	3
21	GPIO12	AC34	inout	3	**22**	GND			
23	GPIO14	AC33	inout	3	**24**	EXP_PLL_P	AJ34	in	3
25	GPIO16	AD34	inout	3	**26**	EXP_PLL_N	AK34	in	3
27	GPIO18	AD33	inout	3	**28**	GND			
29	GPIO20	AE34	inout	3	**30**	GPIO13	AL32	inout	3
31	GPIO22	AE33	inout	3	**32**	GPIO15	AL34	inout	3
33	GPIO24	W31	inout	3	**34**	GPIO17	AL33	inout	3
35	GPIO26	W32	inout	3	**36**	GPIO19	AF31	inout	3
37	GPIO28	Y31	inout	3	**38**	GPIO21	AK31	inout	3
39	GPIO30	Y32	inout	3	**40**	GPIO23	AK32	inout	3
41	GPIO32	AA30	inout	3	**42**	GPIO25	AL31	inout	3
43	GPIO33	AA31	inout	3	**44**	GPIO27	AM32	inout	3
45	GPIO34	AB31	inout	3	**46**	RFU	RFU	RFU	NA
47	GPIO35	AB32	inout	3	**48**	GPIO31	AM30	inout	3
49	GPIO36	AB30	inout	3	**50**	GPIO37	AN34	inout	3
51	GPIO38	AC30	inout	3	**52**	GPIO39	AN33	inout	3
53	GPIO40	AD30	inout	3	**54**	GPIO41	AP33	inout	3
55	GPIO42	AD31	inout	3	**56**	GPIO43	AP32	inout	3
57	GPIO44	AE31	inout	3	**58**	GPIO45	AP31	inout	3
59	GPIO46	AE32	inout	3	**60**	GPIO47	AP30	inout	3

The bank 0 contains 3.3V power and ground pins, 48 general purpose IO (GPIO) pins, and dedicated clock input pins (EXP_PLL_P and EXP_PLL_N). The clock input pins connect to the PLL input.

Strongly recommended: The clock input to be used is EXP_PLL_P.

Note: GPIO29 is RFU and is not to be used in design.

Table 25: Expansion connector #1 Bank 1 pinout and FPGA mapping

EXP Pin	Function	FPGA pin	FPGA dir	Bank/ SERDES	EXP pin	Function	FPGA pin	FPGA dir	Bank/ SERDES
61	SERDES	PCSC_HDOUTN0	out	PCSC	**62**	SERDES	PCSC_REFCLKN	in	PCSC
63	SERDES	PCSC_HDOUTP0	out	PCSC	**64**	SERDES	PCSC_REFCLKP	in	PCSC
65	GND				**66**	GND			
67	SERDES	PCSC_HDOUTN1	out	PCSC	**68**	SERDES	PCSC_HDINN0	in	PCSC
69	SERDES	PCSC_HDOUTP1	out	PCSC	**70**	SERDES	PCSC_HDINP0	in	PCSC
71	GND				**72**	GND			
73	SERDES	PCSC_HDOUTN2	out	PCSC	**74**	SERDES	PCSC_HDINN1	in	PCSC
75	SERDES	PCSC_HDOUTP2	out	PCSC	**76**	SERDES	PCSC_HDINP1	in	PCSC
77	GND				**78**	GND			
79	SERDES	PCSC_HDOUTN3	out	PCSC	**80**	SERDES	PCSC_HDINN2	in	PCSC
81	SERDES	PCSC_HDOUTP3	out	PCSC	**82**	SERDES	PCSC_HDINP2	in	PCSC
83	GND				**84**	GND			
85	SERDES	PCSA_REFCLKN	in	PCSA	**86**	SERDES	PCSC_HDINN3	in	PCSC
87	SERDES	PCSA_REFCLKP	in	PCSA	**88**	SERDES	PCSC_HDINP3	in	PCSC
89	GND				**90**	GND			
91	SERDES	PCSA_HDOUTN0	out	PCSA	**92**	SERDES	PCSA_HDINN0	in	PCSA
93	SERDES	PCSA_HDOUTP0	out	PCSA	**94**	SERDES	PCSA_HDINP0	in	PCSA
95	GND				**96**	GND			
97	SERDES	PCSA_HDOUTN1	out	PCSA	**98**	SERDES	PCSA_HDINN1	in	PCSA
99	SERDES	PCSA_HDOUTP1	out	PCSA	**100**	SERDES	PCSA_HDINP1	in	PCSA
101	GND				**102**	GND			
103	SERDES	PCSA_HDOUTN2	out	PCSA	**104**	SERDES	PCSA_HDINN2	in	PCSA
105	SERDES	PCSA_HDOUTP2	out	PCSA	**106**	SERDES	PCSA_HDINP2	in	PCSA
107	GND				**108**	GND			
109	SERDES	PCSA_HDOUTN3	out	PCSA	**110**	SERDES	PCSA_HDINN3	in	PCSA
111	SERDES	PCSA_HDOUTP3	out	PCSA	**112**	SERDES	PCSA_HDINP3	in	PCSA
113	GND				**114**	GND			
115	5V				**116**	5V			
117	5V				**118**	5V			
119	5V				**120**	5V			

4.11.2 EXP #1

Expansion connector #1 is the Samtec QSH-030-01-L-D-A high-speed mezzanine connector, marked J13. It mates with the QTH-030 connector, with the recommended mating height of 8mm or more (set by the choice of the QTH-060 connector). This expansion connector is dedicated to the general purpose IO pins. It also comprises 2 dedicated pins for system I2C.

Table 26: Expansion connector #1 pinout and FPGA mapping

EXP Pin	Function	FPGA pin	FPGA dir	Bank	EXP pin	Function	FPGA pin	FPGA dir	Bank
1	5V				**2**	3V3			
3	5V				**4**	3V3			
5	5V				**6**	3V3			
7	SDA	AN32	inout	3	**8**	SCL	AN31	inout	3
9	GPIO48	K33	inout	2	**10**	GPIO49	K30	inout	2
11	GPIO50	K34	inout	2	**12**	GPIO51	K29	inout	2
13	GPIO52	K32	inout	2	**14**	GPIO53	L30	inout	2
15	GPIO54	K31	inout	2	**16**	GPIO55	L28	inout	2
17	GPIO56	L33	inout	2	**18**	GPIO57	L26	inout	2
19	GPIO58	L34	inout	2	**20**	GPIO59	M29	inout	2
21	GPIO60	L32	inout	2	**22**	GPIO61	M28	inout	2
23	GPIO62	L31	inout	2	**24**	GPIO63	M27	inout	2
25	GPIO64	M33	inout	2	**26**	GPIO65	M26	inout	2
27	GPIO66	M34	inout	2	**28**	GPIO67	N30	inout	2
29	GPIO68	M31	inout	2	**30**	GPIO69	N29	inout	2
31	GPIO70	M30	inout	2	**32**	GPIO71	N28	inout	2
33	GPIO72	N33	inout	2	**34**	GPIO73	N27	inout	2
35	GPIO74	N34	inout	2	**36**	GPIO75	R31	inout	2
37	GPIO76	N32	inout	2	**38**	GPIO77	R30	inout	2
39	GPIO78	N31	inout	2	**40**	GPIO79	R28	inout	2
41	GND				**42**	GND			
43	EXP2_PCLK_P	U26	inout	2	**44**	EXP2_PLL_P	V34	in	2
45	EXP2_PCLK_N	U27	inout	2	**46**	EXP2_PLL_N	V33	in	2
47	GND				**48**	GND			
49	GPIO80	P33	inout	2	**50**	GPIO81	R27	inout	2
51	GPIO82	P34	inout	2	**52**	GPIO83	T32	inout	2
53	GPIO84	R33	inout	2	**54**	GPIO85	T31	inout	2
55	GPIO86	R34	inout	2	**56**	GPIO87	T30	inout	2
57	GPIO88	T33	inout	2	**58**	GPIO89	T29	inout	2
59	GPIO90	T34	inout	2	**60**	GPIO91	U32	inout	2

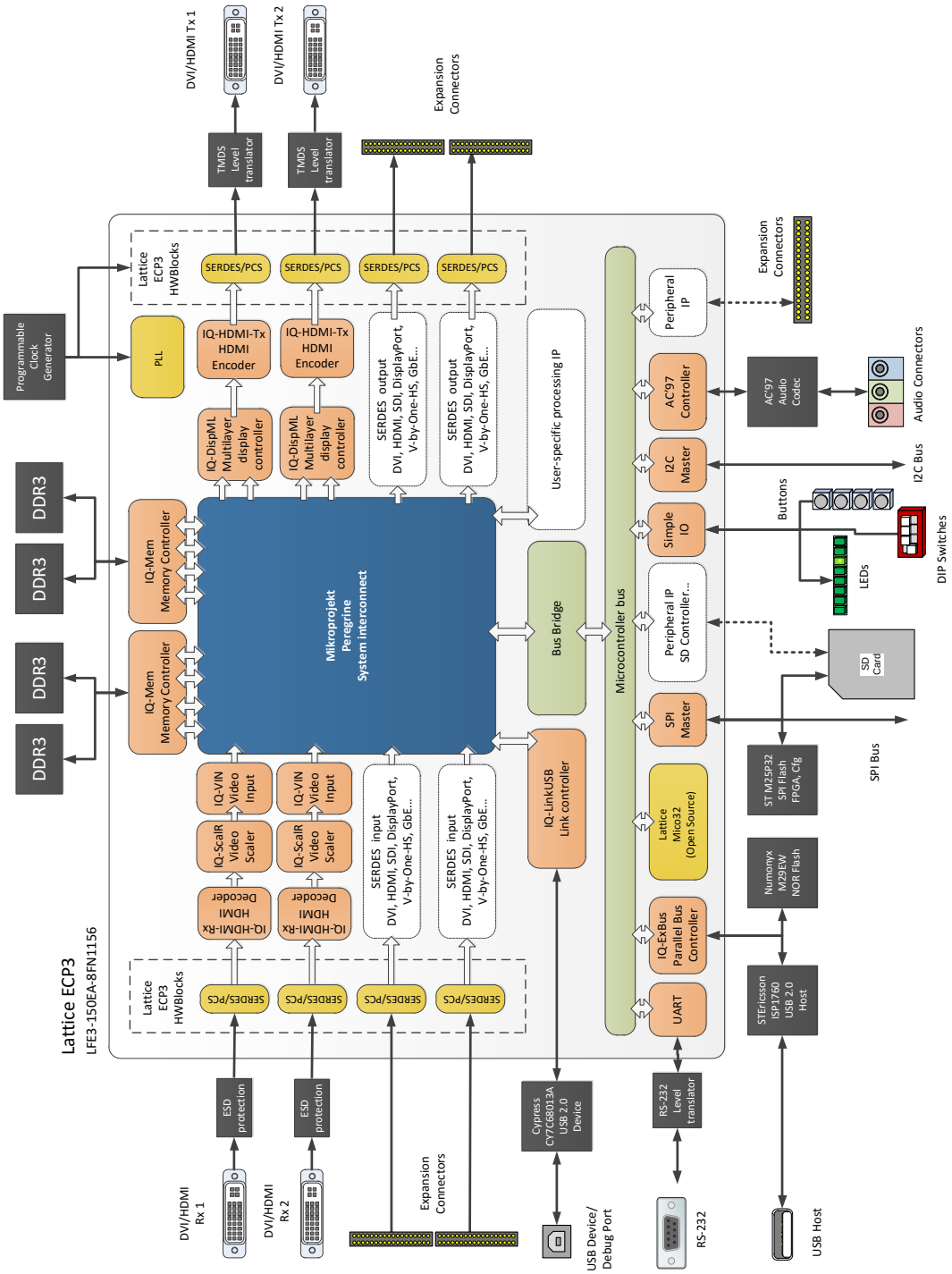
4.11.3 EXP #2

Expansion connector #2 is the 15x2 header with the 2.54 mm pitch (100 mils), marked J14. It features 22 generic IO pins (HDR_IOx), 3.3V and 5V power supplies.

Table 27: Expansion connector #2 pinout and FPGA mapping

EXP Pin	Function	FPGA pin	FPGA dir	Bank	EXP pin	Function	FPGA pin	FPGA dir	Bank
1	GND				**2**	GND			
3	5V				**4**	3V3			
5	HDR_IO0	B28	inout	1	**6**	HDR_IO1	A28	inout	1
7	HDR_IO2	A27	inout	1	**8**	HDR_IO3	C27	inout	1
9	HDR_IO4	B27	inout	1	**10**	HDR_IO5	D27	inout	1
11	HDR_IO6	A26	inout	1	**12**	HDR_IO7	D26	inout	1
13	HDR_IO8	C26	inout	1	**14**	HDR_IO9	E27	inout	1
15	HDR_IO10	A25	inout	1	**16**	HDR_IO11	C25	inout	1
17	HDR_IO12	B25	inout	1	**18**	HDR_IO13	D25	inout	1
19	HDR_IO14	A24	inout	1	**20**	HDR_IO15	D24	inout	1
21	HDR_IO16	B24	inout	1	**22**	HDR_IO17	E24	inout	1
23	HDR_IO18	A23	inout	1	**24**	HDR_IO19	C23	inout	1
25	HDR_IO20	B23	inout	1	**26**	HDR_IO21	D23	inout	1
27	3V3				**28**	5V			
29	GND				**30**	GND			

5 SoC Architecture



5.1 Basic architecture

The basic architecture of the Sparrowhawk FX SoC is built around Mikroprojekt's IQ-Video video processing solution, based on the Peregrine system interconnect.

5.1.1 Peregrine system interconnect

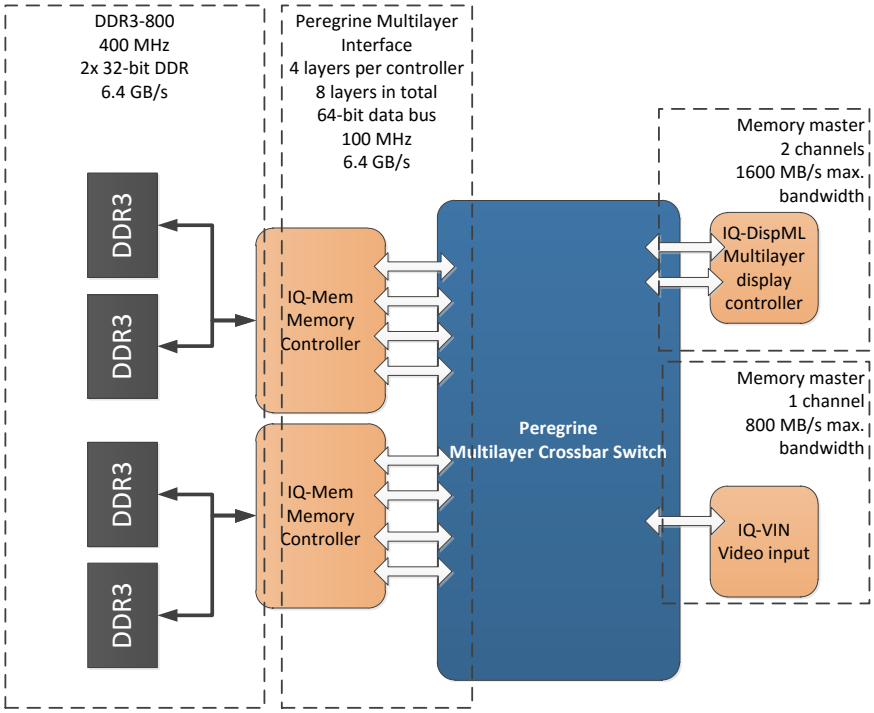


Figure 9: The Peregrine System Interconnect Architecture

The Peregrine system interconnect architecture is Mikroprojekt's answer to the bandwidth issues in high performance video applications on FPGAs. The Peregrine bus is a multi-layered crossbar switch allowing the connection of multiple bus masters to bus slaves over multiple data channels, reducing bus congestion and allowing higher throughputs.

The bus transactions are optimized for long sequential burst accesses commonly encountered in video applications. The memory controller is a vital part of the architecture, providing multiple separated access channels, which additionally allow for zoning and hardware decoupling of individual bandwidth utilization regimes, to ensure the maximum efficiency of operations on the memory

interface. The memory controllers also integrate intelligent arbiters which optimize the order of accesses received over the multiple channels.

The Peregrine crossbar switch allows multiple masters to be connected to the memory over multiple layers. The total number of master channel connections can be greater than the number of slave channels. The Peregrine crossbar switch performs access arbitration between multiple masters. The arbiter can be programmed either to ensure priority and/or fairness between multiple masters.

The total delivered bandwidth to a single master is limited by the number of individual channel it can access. In the proposed configuration, each channel can deliver 800 MB/s of bandwidth, which is sufficient to simultaneously input and output one 1920x1080 full HD video stream at 60Hz.

5.2 Memory

The DDR3 memory is connected in the 2x2 configuration, enabling simultaneous use of all chips by controlling them with 2 IQ-Mem multi-channel memory controllers, both operating on the 400 MHz clock and 32-bit memory data bus. Available theoretical bandwidth is therefore 6.4GB/s, utilized by the IQ-Mem with more than 90% efficiency (depending on the use case).

In order to utilize the full potential of the DDR3-800, IQ-Mem is designed as a multi-channel memory controller, enabling simultaneous memory access to multiple bus masters, one on each channel. This feature uses multi-layer capability of the Peregrine crossbar switch, and utilizes separate read and write FIFOs (two per channel) for completely decoupling the bus operation and memory operation. The bus performance is further improved by using the Peregrine capability to simultaneously transfer write and read data.

5.3 Video out

Video output is handled by Mikroprojekts IQ-HDMI-Tx and IQ-DispML IP Cores, enabling the driving of various display systems and panels through DVI/HDMI. The IQ-DispML display controller can also be used to drive a panel directly, through one of the expansion connectors available on the PCB. Video clock can be synthesized by the Si5338 programmable clock generator, capable of

generating 2 separate video clocks. Si5338 is configurable through I2C interface, using IQ-I2C I2C bus controller.

The IQ-DispML IP core allows mixing of video streams of various resolutions and color depths, combining multiple image layers into one output image with windowing, alpha blending and per-pixel transparency. IQ-DispML supports SW configuration of all display parameters except clock frequency, enabling use of most of the displays available on the market.

The output of the IQ-DispML can be connected to the IQ-HDMI-Tx encoder, capable of encoding standard video signals into the 3x10-bit words using TMDS encoding. These signals are connected directly to the SERDES and drive the DVI output, by using another channel for clock generation.

5.4 Video in

The solution integrates IQ-HDMI-Rx, IQ-VIN and IQ-ScalR IP cores for video reception. IQ-HDMI-Rx decodes the HDMI output and outputs the DVI/HDMI video data, audio and info frames to the IQ-VIN. Besides IQ-HDMI-Rx, various video decoders can be connected to the IQ-VIN, using one of the expansion connectors.

Within the IQ-VIN, the video data is first driven into the integrated IQ-ScalR IP core, where optional image scaling is supported, and one or more additional processing modules conforming to a standard interface. The HDMI audio data is bypassed directly to the output stage. Additional processing modules can be integrated into the datapath.

The output stage performs the final data encoding and transmits the video data to the memory, with support for various memory configurations (stripe and addressing, interleaving) and frame handling (frame skip).

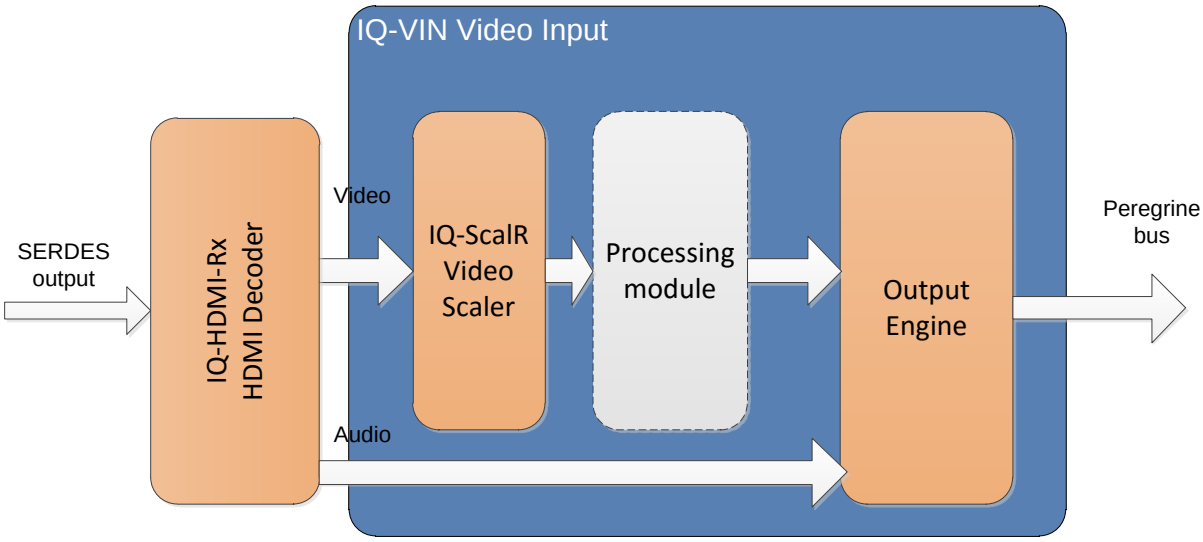


Figure 10: Video input processing

5.5 Peripherals

External connectivity to other systems is provided through several interfaces.

5.5.1 IQ-LinkUSB USB slave controller

The IQ-LinkUSB is an interface controller serving as a bus master on the Peregrine bus, performing operations delivered over the IQ-Link protocol from the external USB interface. The USB interface operation is handled through a Cypress CY7C68013A USB controller, integrating an 8051 microcontroller core to handle USB protocol requests, and providing a high-speed endpoint FIFO interface which allows high-bandwidth USB 2.0 transfers up to 30 MB/s delivered by the bulk endpoint transfers.

Single and burst read and write transfers can be issued by the USB host, which are executed on the Peregrine bus, with the results subsequently transferred back to the host.

The IQ-LinkUSB is employed as a debug and control link. The high bandwidth of USB 2.0 allows:

- download of test images and data,
- memory readback of various intermediate processing results

- run-time reconfiguration and download of software
- register setting and readout
- complete solution control

5.5.2 UART

The UART interface is a standard UART supporting speeds up to 115200 bps with hardware flow control on RS-232, or up to 3 Mbps for IrDA or other application. One RS-232 interface is included on the Sparrowhawk FX board, and is under control of the embedded microcontroller. Additional UART interfaces can be added using expansion connectors.

5.5.3 I2C

Standard I2C bus controller is integrated and controls clock generator Si5338 and any device connected to the expansion connectors. It is controlled by the embedded microcontroller.

5.5.4 SPI

An SPI master controller is embedded to support access and programming of the onboard SPI flash and the SD card. The master supports SPI access in all 4 modes with frequencies up to 50 MHz. Optionally, it can be expanded to support quad-speed SPI or higher frequencies.

5.5.5 Buttons, switches and LEDs

The system integrates 8 status LEDs, 4 DIP-style switches and 4 push buttons.

Leds are turned on by writing '1' to a control register, and turned off by writing '0'. After FPGA boot, all LEDs are turned off.

DIP switches are connected to pull-down RC network, when switch is open, FPGA has '0' on input, when switch is closed FPGA has '1' on input.

Push-button switches are connected to pull-down RC network, when switch is open, FPGA has '0' on input, when switch is closed FPGA has '1' on input.

LEDs, buttons and switches are controlled by the embedded microcontroller.

5.6 Nonvolatile storage

Several nonvolatile storage devices are supported:

5.6.1 Numonyx Axcell M29EW NOR Flash

The board integrates a parallel asynchronous NOR flash for storage of bulk data with fast access, such as test images, splash screens, and microcontroller software. The internal flash controller supports fast page read mode to extract maximum reading performance, up to 30 MB/s. TrueFFS flash file system implementation is feasible on the device.

5.6.2 SD Card slot

Secure digital cards (SD/SDHC/SDXC) are supported on the Sparrowhawk FX board, and a slot is present on the board. The default access method is through the SPI bus. Additionally, a SD controller IP core can be integrated to support high-speed data reads and writes. SD cards support multi-gigabyte storage for embedded video and graphics.

5.6.3 SPI Flash

An ST M25P64 SPI flash is connected to the FPGA. This device serves as the FPGA design storage, and can be accessed for field updates of the board's FPGA over software. Additionally it can hold an additional "safe" FPGA image for dual boot, software for an embedded microprocessor, or application-specific data.

5.6.4 USB Host

Optionally, USB mass storage devices can be supported through the onboard USB 2.0 host, ISP1760. The device shares the same parallel bus with the M29EW parallel flash, so the same controller, IQ-ExBus is used for accessing both devices.

5.7 Audio

Audio IO is supported on the Sparrowhawk FX PCB by an AC'97 codec WM9707. The device supports analog line-in, analog line-out and digital output S/PDIF. WM9707 is controlled by the embedded microcontroller.

5.8 Embedded Microcontroller

5.8.1 Hardware description

The embedded microcontroller is a Lattice Mico32 32-bit Harvard RISC microprocessor. The processor is optimized for Lattice FPGA devices. It has 32 32-bit general purpose registers. The processor employs a 6-stage pipeline for higher throughput, and achieves up to 115 MHz within the Lattice ECP3.

For highly embedded operations, or to accelerate certain applications, Inline memory can be attached to the processors for fast access, avoiding the cache. Both instruction and data inline memory is supported.

The processor is available in multiple configurations, ranging from Basic, highly embedded version with no multipliers, caches and pipelined shifters, Standard, with no caches, but fully pipelined and with hardware multipliers, and Full, with caches added.

The implementation data for Standard and Full configurations is given in **Error! Reference source not found.**. Beside the numbers is the total percentage of the ECP3-150 resources.

Table 28: FPGA utilization of Mico32 CPU variants usable for computation

Version	LUT4s	REGs	MULs	ALUs	EBRs
Standard	2702(2%)	1296(1%)	8(1%)	4(1%)	4(1%)
Full	3361(3%)	1645(2%)	8(1%)	4(1%)	14(4%)

The microcontroller is sufficiently small to facilitate use of multiple processors embedded.

5.8.2 Functionality

The Software embedded in the primary microcontroller controls the overall system, providing control for:

- device power-up
- system state
- initialization of hardware such as video inputs, display controllers and video processors
- ddc readout
- service and test patterns
- UART communication

A bootloader can be programmed in the SPI flash or NOR flash and loaded on system startup, after which the microcontroller can load additional software and data from other nonvolatile storage.

6 Default demo application

The default demo application enables mixing of two video streams with the overlay of graphic content. Several functionalities are demonstrated in the course of the demo.

6.1 Display driving

The board will communicate with a connected display over the DVI interface, reading out the EDID and configuring the output for the appropriate resolution and timing. The display will be powered up and a color bar pattern will be shown indicating that the display is properly driven.

The following resolutions are supported in various timings:

- 640x480
- 800x600
- 1024x600
- 1024x768
- 1280x720
- 1366x768
- 1280x1024
- 1600x1200
- 1680x1050
- 1920x1080

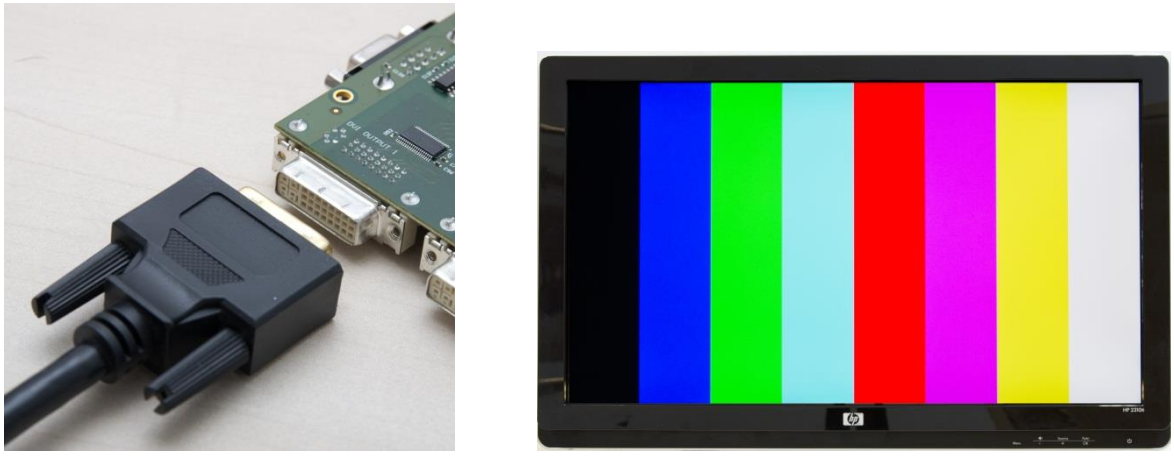


Figure 11: Display driving feature

The color bar pattern should cover the full screen with color bars of equal width. The colors are, in order from left to right:

Table 29: Demo color bar pattern

Black	Blue	Green	Cyan	Red	Magenta	Yellow	White
#000000	#0000FF	#00FF00	#00FFFF	#FF0000	#FF00FF	#FFFF00	#FFFFFF

6.2 Graphics overlay

The IQ-DispML IP Core can handle multi-layer graphics output with transparency and scrolling effects. Pressing the button SW2 enables a scrolling ticker overlay and a logo overlay on the displayed image.

Figure 12: Logo and ticker graphics overlay

The logo and ticker can be turned on or off at any time. If there is a video stream present, the stream will be scaled down gradually (non-aspect ratio) to accommodate the scrolling ticker.

6.3 Video input

The IQ-VIN IP core captures the video stream input to the DVI input connector. The input EDID is set according to the output resolution. The embedded

firmware will automatically display the incoming video stream once a cable is connected to the DVI input.

The default input shown after power-up is the DVI input #0.

Figure 13: Video input

6.4 Video overlay / Picture-in-Picture

The video stream on video input #1 can be overlaid on video input #0 or vice versa in real time. This is shown in a "PIP" (picture in picture) demo mode. The PIP mode is activated by pressing SW3 once.

Figure 14: PIP Demo mode

The video window will appear on the left side of the screen and show real-time feed from DVI input #1.

A subsequent press to SW3 will trigger an animation where the overlay window will gradually move from the left to the right side of the window and gain 50% transparency, so that the video underneath is visible through the video above. A third press to SW3 will fade out the overlay video.

6.5 Fade-in, Fade-out and swap

Fade-in and fade-out effects are used throughout the demo. They can be readily shown when swapping the video channels by pressing SW4. A single press to SW4 will swap the two video streams in any mode.

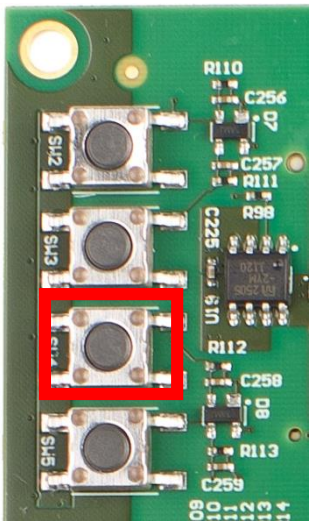


Figure 15: Swap video sources control

6.6 Arbitrary scaling and side by side display

IQ-VIN IP cores and IQ-ScalR scalers allow arbitrary frame by frame scaling with varying scaling factors for both horizontal and vertical axes. This can be easily demonstrated by pressing the SW5 button. On pressing SW5, the demo will transit to the "SbS" (Side by side) mode.

On entering this mode, the currently fullscreen input will scale down to 50% size in both directions with preservation of aspect ratio, to the left side of the screen. The other video input will fade in beside on the right side.

Figure 16: Side by side mode

Pressing SW5 again will turn off the SBS mode. Upon turning off, the right image will fade out. Afterwards, the left image will scale up to 100%, first in vertical, then in horizontal direction, without constraining to the image aspect ratio.

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