IQ-DispLite-Lightweight Configurable Display Controller

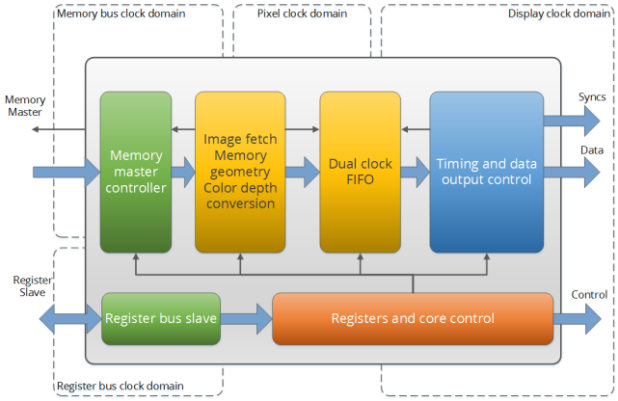
Description

The IQ-DispLite is a lightweight, fully software configurable display controller IP core. It performs continuous refresh of graphical flat panel displays (TFT LCD, AMOLED) from a designated frame buffer located in a memory device mapped to the system bus. SDRAM and SRAM devices are supported as frame buffers, depending on the bandwidth requirements.

IQ-DispLite is designed to provide an optimum tradeoff of performance and resource utilization in FPGA devices while retaining a high degree of configurability.

The IP core can be additionally scaled down at compile time by reducing bus widths and fixing timing parameters, allowing the user to fully optimize the IQ-DispLite for a specific configuration.

Block Diagram



Implementation

Altera Cyclone III

EP3C10				
LEs	BRAMs (M9K)	MULs	IO*	F_{max}**
1316	3	0	252	154 MHz

Lattice ECP3

LFE3-35EA					
Registers	LUT4s	EBRs	MULs	IO*	F_{max}**
952	1355	3	0	252	178 MHz

* assuming all core ports are routed off chip
** maximum frequency of the system bus interface

Applications

- Vending machines
- Video monitors
- Automotive infotainment
- Medical instrumentation
- Human machine interface (HMI) systems
- Mobile devices

Deliverables

- Encrypted RTL source code supporting SOPC builder (Altera) / Precompiled IP core in desired configuration (Lattice)
- Testbench
- Datasheet
- User manual
- Implementation guide

Verification

The core has been rigorously tested in functional simulation and actual hardware. The core is accompanied with an automated testbench with a display simulation model and a memory simulation model. The memory model can be initialized with the desired bitmap through simple software provided with the model.

Features

- Fully programmable clock and timing control for flat panel displays with progressive scanning
- Support for resolutions up to 4096x4096
- Completely variable timing parameters, for standard or specific display resolutions
- Support for 8,16, 18 or 24 bit RGB output color depth
  - *8-bit RGB (3:3:2)*
  - *16-bit RGB (5:6:5)*
  - *18-bit RGB (6:6:6)*
  - *24-bit RGB (8:8:8)*
- Standard or multiplexed display data bus
- Display power control lines
- Interrupt generation on vertical sync for software synchronization
- Frame buffer management
  - Double buffering to reduce image flicker
  - Variable frame buffer organization with software-configurable memory stripe
  - Image scroll via unconstrained frame buffer addressing
  - Frame buffer color depth support:
    - *8 bit RGB (3:3:2)*
    - *16 bit RGB(5:6:5)*
    - *24 bit RGB(8:8:8)*
- Compile-time configuration for reducing resource cost by fixing parameters
- Support for multiple clock domains to ease timing closure
- Integrated DMA memory master supporting low-overhead burst transfers
  - Master bus interfaces
    - *AMBA AHB*
    - *AMBA AXI4*
    - *Avalon*
    - *Peregrine**

* Peregrine bus is Mikroprojekt's proprietary bus architecture, optimized for FPGA architecture

- Configuration bus slave interface with address-mapped registers
  - Slave bus interfaces
    - AMBA APB
    - Avalon

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