IQ-LinkSPI – Frame-based wrapper for the SPI

Description

IQ-LinkSPI is a frame-based wrapper for the SPI interface. It is designed to receive frames containing commands for the bus operations and the wrapper configuration.

All frames are confirmed by an answering frame. The commands are identified by a 3-bit tag, and all frames are protected from error by a 16-bit CRC (CCITT).

IQ-LinkSPI doesn't check for the compatibility with the system bus, so the SPI master should send only commands which conform to the bus specification.

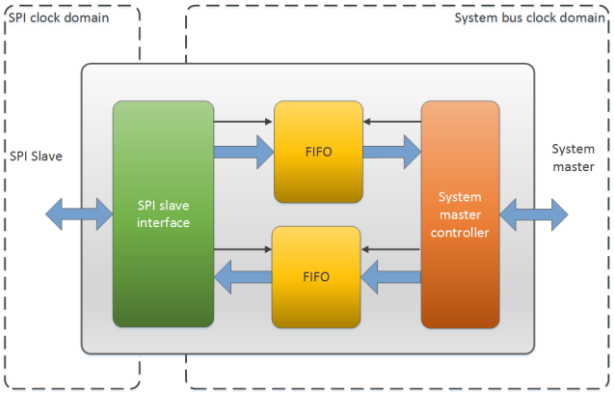
Applications

- Vending machines
- Video monitors
- Human machine interface (HMI) systems
- Industrial control and monitoring

Deliverables

- Precompiled IP core in desired configuration
- Testbench
- Datasheet
- User manual
- Implementation guide

Block Diagram



Implementation

Altera Cyclone III

EP3C10				
LEs	BRAMs (M9K)	MULs	IO*	F_{max}**
892	2	0	119	162 MHz

* assuming all core ports are routed off chip

** maximum frequency of the system bus interface

Verification

The core has been rigorously tested in functional simulation and actual hardware. The core is accompanied with an automated testbench with an SPI master simulation model and a memory simulation model. The memory model can be initialized with the desired data using the standard memory initialization file.

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Features

- Configurable SPI mode of operation and chip select polarity
  - *Mode 0 (CPOL=0, CPHA=0)*
  - *Mode 1 (CPOL=0, CPHA=1)*
  - *Mode 2 (CPOL=1, CPHA=0)*
  - *Mode 3 (CPOL=1, CPHA=1)*
- Detection of errors using a 16-bit CRC (CCITT).
- Decoupled command and response interfaces, allowing for high efficiency of the communication.
- FIFO-based interface with configurable depth, allowing a trade-off between resource use and maximum number of commands issued before receiving responses.
- Easy adaptation to the various FPGAs and various design requirements (ranging from slow, low-budget interfaces to the high bandwidth applications)
- Integrated DMA memory master supporting low-overhead burst transfers
  - *Master bus interfaces*
    - *AMBA AHB*
    - *Avalon*

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