

KONDOR AX

Advanced System Development Board

COMMS DEMO GUIDE

UM0032

Rev. 1.2

5.11.2015.

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Revision History

Revision	Date	Author	Modification
1.0	28.10.2015.	NDZ	Initial
1.1	2.11.2015.	NDZ	Software preparations changed
1.2	5.11.2015.	NDZ	Organization structure edited

Related Documents

ID	Code	Description
1	UM0026	KONDOR AX – User's Manual
2	UM0027	KONDOR AX – Linux BSP Build Setup Guide
3	UM0033	KONDOR AX – Comms Demo Reference Design Guide

1 Introduction

This demo shows some of Kondor AX communication capabilities, demonstrated with two Kondor AX boards, along with other additional hardware.

2 Hardware preparations

For this demo, two Kondor boards with required DAC and ADC boards must be properly connected and prepared, and contain the standard Linux distribution prepared by Mikroprojekt.

2.1 Hardware requirements

- 2x Kondor AX Development Board with Lattice LFE5UM-85F FPGA device
- 2x 12V DC power supply for the Kondor AX Board
- Texas Instruments DAC37J82 EVM (DAC3XJ8X EVM)
- Texas Instruments ADS42JB69 EVM
- 2x 5V DC power supply for TI boards
- SMA cable for analog loopback
- 2x Finisar's FTLF1326P3BTL CPRI SFP+ transceivers
- 1x LC/LC Duplex 9/125 Single mode Fiber Optic Cable (DK-2933-01) for CPRI loopback

2.2 Before powering up the boards

On ADS42JB69 board:

1. move SJP4 - SJP11 to shunt pins 1 and 2 to select FMC interface instead of USB for SPI communication,
2. remove the following pull-down resistors: R99, R100, R103, R104.

On DAC37J82 board:

1. Short 1-2 of JP3 to select FMC connector as SPI signal source.

On Kondor AX boards:

1. Short 1-2 of J16 on the Kondor AX board connected to the ADC board
2. Short 2-3 of J16 on the Kondor AX board connected to the DAC board
3. To select interfaces to SerDes lanes, place capacitors of the passive capacitor mux in the following positions:

Table 1: Selected SerDes interfaces defined by capacitor position in passive network

Lane	Passive Designator	Network	Capacitor position	Selected Interface
L0_TX	U38/U36		3-2	FMC connector
L0_RX	U35/U37		3-2	FMC connector
L2_TX	U40/U42		1-2	SFP cage 0
L2_RX	U39/U41		1-2	SFP cage 0
Dual DCU0 reference clock	U47/U48		3-2	FMC connector

2.3 Connecting the boards

Connect the DAC37J82 board and Kondor AX board via the FMC connector.

Connect the ADS42JB69 board and Kondor AX board via the FMC connector.

Connect SMA Cable to DAC37J82 J2 output connector and to the ADS42JB69 J1 input connector.

Insert CPRI SFP+ transceivers in the J9 SFP cage of each Kondor AX board and connect them via optical cable.

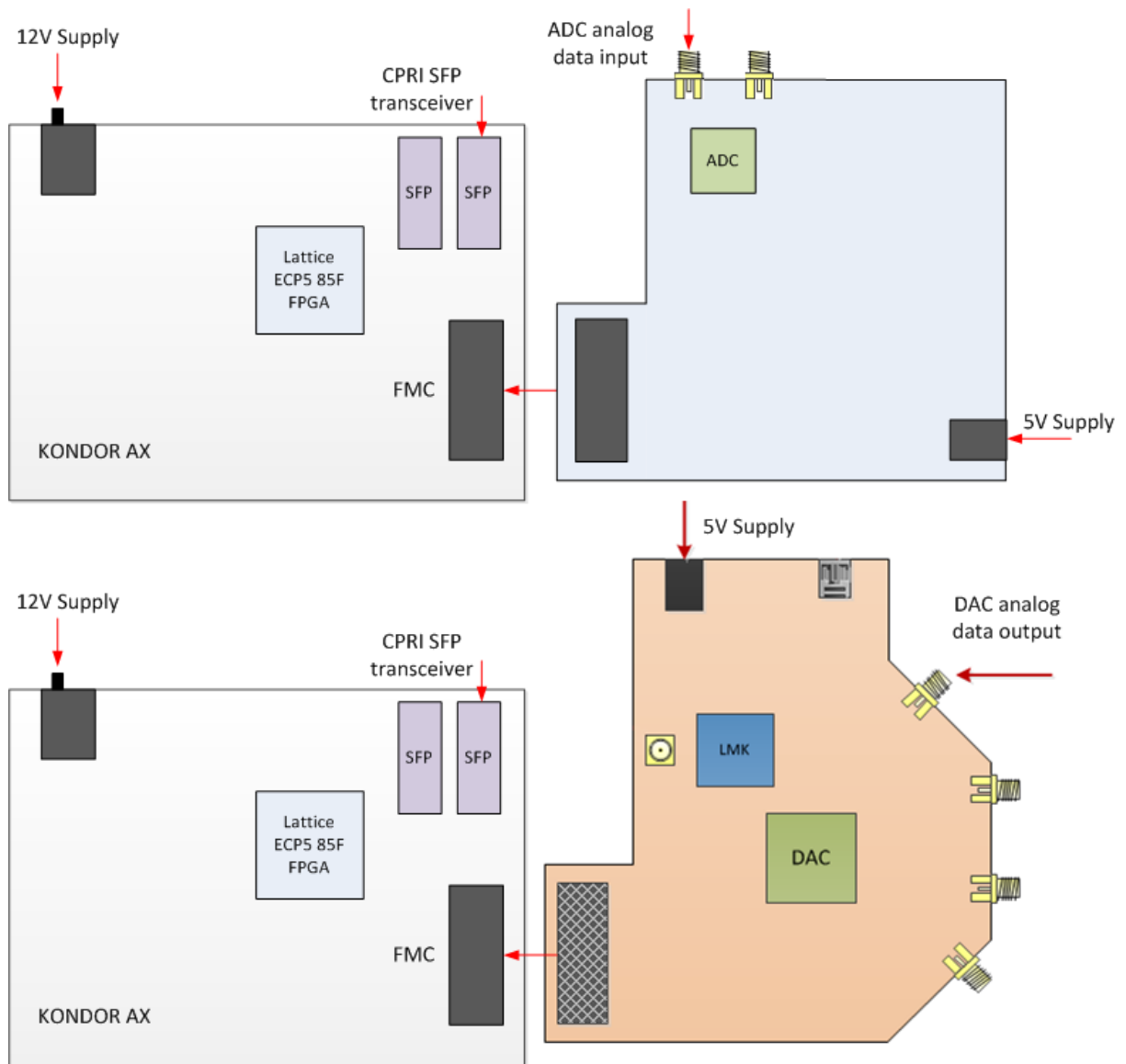


Figure 1: Demo setup block schematic

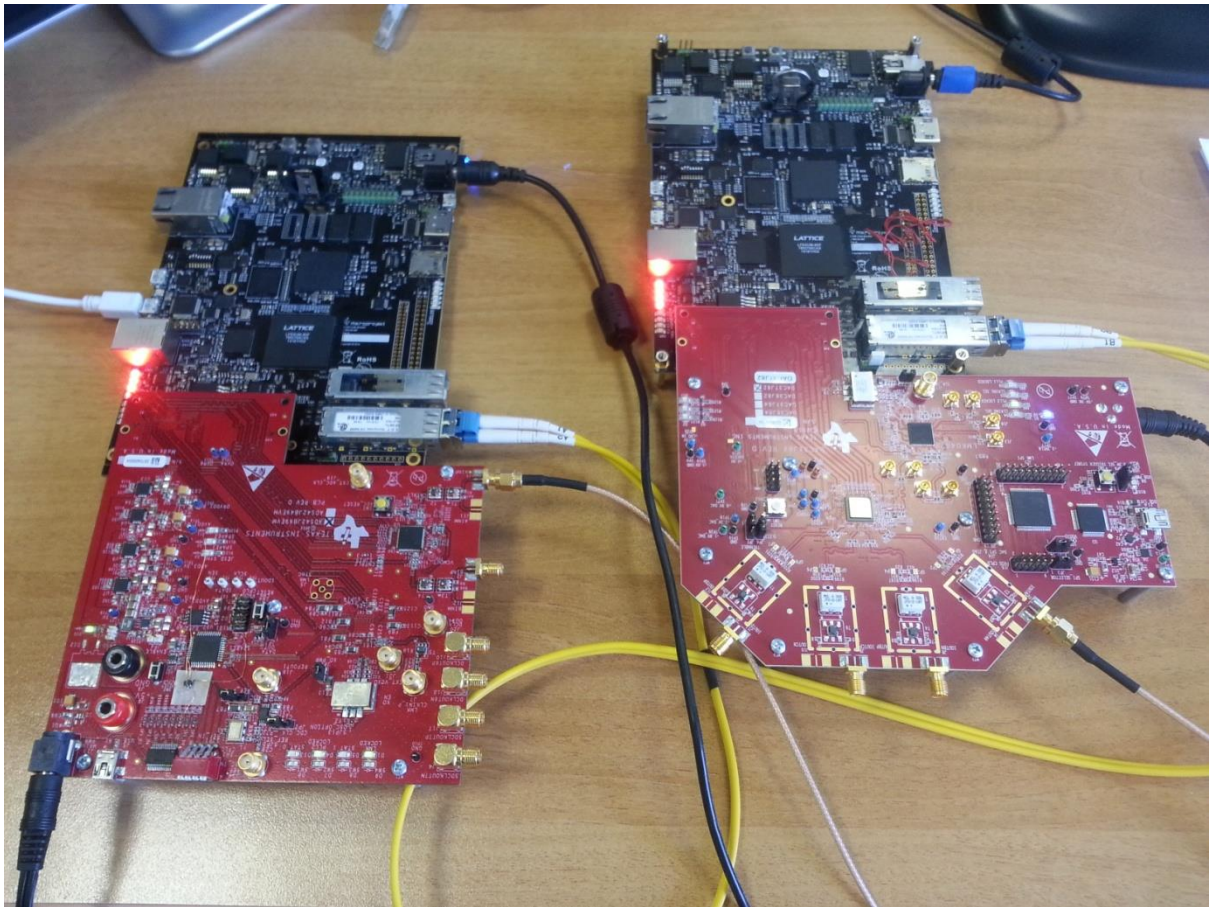


Figure 2: Demo setup

2.4 Power up sequence

For the proper operation of the Comms Demo, please follow the following power up sequence:

1. To power on the DAC37J82 board, connect 5V DC power supply to connector J23.
2. Power on the Kondor AX board connected to DAC37J82 by connecting 12V DC (1.5 A) power supply and pressing S1 switch to apply power.
3. Power on the ADS42JB69 board by connecting 5V DC power supply to connector J13.
- 4. Press SW1 to reset the ADC!!**
5. Power on the Kondor AX board connected to ADS42JB69 by connecting 12V DC (1.5 A) power supply and pressing S1 switch to apply power.

3 Downloading FPGA design

This is one option of downloading FPGA design using provided .bit files. As .sea and .sed files are also provided, the alternative option of downloading FPGA design will be described in following chapters. For option including .bit files, follow next steps for each of two Kondor AX boards:

1. Connect micro USB cable to U33 connector on the board, install necessary USB/serial port drivers on the PC if required.
2. Start **Lattice Diamond Programmer** tool and select matching communication port for transferring data to the board.
3. **Device Family** should be **ECP5UM**; **Device** should be **LFE5UM-85F**.
4. Double click on the cell in **Operation** column to open **Device properties** dialog box. Set **Access mode** to **JTAG 1532 Mode**; set **Operation** to **Fast Program**.
5. Under **Programming file**, select the desired .bit file containing FPGA design.
6. Close the dialog box by clicking **OK**.
7. **Menu Design** → **Program**.

4 Software preparations

Both Kondor AX boards need to be configured separately.

Kondor board can be operated using a terminal application on PC. Connect PC to U24 connector on Kondor board using a micro USB cable. Board should be recognized by OS as a virtual port. Start a terminal application (e.g. Tera Term) on PC, choose appropriate virtual port and baud rate 115200 bps. Login using:

```
> root
```

Before downloading files, it is advisable to create a new folder where they should be downloaded. Assuming the name of the folder will be comms_demo, located inside /ecp5com/demos folder, next command should be written:

```
> mkdir /ecp5com/demos/comms_demo
```

Go to the folder with:


```
> cd /ecp5com/demos/comms_demo
```

Once positioned in newly created folder, download all .ko and .lxe files from provided demo ZIP file.

The easiest way to download necessary files is to use ZModem option in Tera Term. Select **File** → **Transfer** → **ZModem** → **Send** and browse for all files needed. Multiple file download (at once) is possible.

For executable files (.lxe), after transfer also do:

```
> chmod +x *.lxe
```

Though the easiest, the above mentioned way is not the fastest, so an alternative download option using file web server (e.g. Mongoose) is described Kondor Ax – User's Manual.

*Note: optionally, to avoid switching micro USB cable from one board to another, two cables and two terminal application windows can be used instead. Just be careful not to mix up terminal windows.

5 Demo

For this demo, working folder will be /ecp5com/demos/comms_demo folder (i.e. folder where files are downloaded), containing all necessary files for use. Two tests can be done: CPRI to JESD204B bridge and CPRI over Ethernet.

5.1 Design download

If FPGA designs are not yet downloaded, besides procedure described in chapter 3, Slave SPI binaries (.sea and .sed files) can be used instead.

5.1.1 DAC side

Download dac_algo.sea and dac_data.sed to working folder according to any of procedures described in chapter 4.

Launch SPI programming application:

```
> ../../sspiem.lxe dac_algo.sea dac_data.sed
```

Programming should last a couple of seconds.

LED D7 on DAC board should be lit after FPGA design is downloaded.

5.1.2 ADC side

Download `adc_algo.sea` and `adc_data.sed` to working folder according to any of procedures described in chapter 4.

Launch SPI programming application:

```
> ../../sspiem.lxe adc_algo.sea adc_data.sed
```

Programming should last a couple of seconds.

LEDs D1 and D4 on ADC board should be lit after FPGA design is downloaded.

5.2 CPRI to JESD204B bridge

In this part of the demo, samples are generated on ADC board and sent to CPRI link. DAC board receives samples over CPRI link and forwards them over JESD to DAC itself. Analogue values are output by the DAC and received by ADC. Finally samples are received and read over JESD on ADC side and displayed, and they should match those initially sent.

5.2.1 Drivers

The same `ecp5com_eim.ko` driver must be loaded on both boards separately.

Before loading driver, any already loaded driver must be unloaded. Use:

```
> lsmod
```

to check if any loaded driver is listed. If so, unload it using:

```
> rmmmod <driver.ext>
```

where `driver.ext` represents driver listed as already loaded. Now, driver necessary for this test can be loaded:

```
> insmod ecp5com_eim.ko
```

Finally, CPRI over SerDes connection has to be checked by running:

```
> ./test_cpri.lxe
```

If message about SerDes status is "serdes 1 link 1", DAC side is ready. If message is different, try to power down all boards and start demo again. If repowering does not help, contact tech support, as it could be design related problem.

5.2.2 Test

Run test_dac.lxe on DAC side using:

```
> ./test_dac.lxe 1 10 10000 2
```

The last number (2) initializes the board to receive samples from CPRI link and forward them to DAC. The DAC board will not generate any samples on its own.

Now run the same file on ADC side:

```
> ./test_dac.lxe 1 10 32767 1
```

The last number (1) instructs the application to send generated samples over CPRI link, instead of directly to DAC.

After test_dac application is run on both boards with appropriate options, finally, test_adc (on ADC side) can be run, and it will receive the same samples. Run:

```
> ./test_adc.lxe 50
```

Optionally, to visually verify JESD, DAC and ADC functionality:

- launch Microsoft Excel or similar application
- copy column of numbers from terminal window attached to ADC board after running test_dac.lxe into Excel and plot a 2D graph - it will show the ideal signal we are telling DAC board to output
- copy column of numbers from terminal window attached to ADC board after running test_adc.lxe into Excel and plot a 2D graph - it will show the signal received by ADC board and should be different than ideal one due to physical limitations, but recognizable

Test can now be repeated by running .lxe applications again and trying different types of signals.

5.3 Ethernet over CPRI

This part of the demo verifies that ARM CPU can access FPGA over EIM interface and use TSMAC core, and that network packets are sent and received by TSMAC over CPRI. Two boards are connected over CPRI link and use TSMACs to send and receive regular IP packets.

5.3.1 DAC side driver

Turn off default network interface by running:

```
> ifconfig eth0 down
```

Before loading ecp5eim.ko driver, any already loaded driver must be unloaded. Use:

```
> lsmod
```

to check if any loaded driver is listed. If so, unload it using:

```
> rmmod <driver.ext>
```

where driver.ext represents driver listed as already loaded. Now, driver necessary for this test can be loaded using:

```
> insmod ecp5eim.ko debug=0 loopback=0 extmode=2 mac_addr=998877665544
```

Bring up new CPRI network interface on DAC board:

```
> ifconfig eth1 up 192.168.2.224
```

5.3.2 ADC side driver

Turn off default network interface by running:

```
> ifconfig eth0 down
```

Before loading ecp5eim.ko driver, any already loaded driver must be unloaded. Use:

```
> lsmod
```

to check if any loaded driver is listed. If so, unload it using:

```
> rmmod <driver.ext>
```

where driver.ext represents driver listed as already loaded. Now, driver necessary for this test can be loaded using:

```
> insmod ecp5eim.ko debug=0 loopback=0 extmode=2 mac_addr=112233445566
```

Bring up new CPRI network interface on ADC board:

```
> ifconfig eth1 up 192.168.2.223
```

5.3.3 Test

Verify network connection really works by detecting ADC board from DAC side:

```
> ping 192.168.2.223
```

During communication between boards, information about data transfer will be written line by line. To stop it, press **Ctrl+C** on the keyboard. Depending on time spent to test the network connection, message about number of packets will be shown. Example of successful test can be seen in Figure 3:

```
root@freescale /ecp5com/demos/comms_demos$ ping 192.168.2.223
PING 192.168.2.223 (192.168.2.223): 56 data bytes
64 bytes from 192.168.2.223: seq=0 ttl=64 time=27.021 ms
64 bytes from 192.168.2.223: seq=1 ttl=64 time=6.867 ms
64 bytes from 192.168.2.223: seq=2 ttl=64 time=6.787 ms
64 bytes from 192.168.2.223: seq=3 ttl=64 time=6.697 ms
64 bytes from 192.168.2.223: seq=4 ttl=64 time=6.631 ms
64 bytes from 192.168.2.223: seq=5 ttl=64 time=6.555 ms

--- 192.168.2.223 ping statistics ---
6 packets transmitted, 6 packets received, 0% packet loss
round-trip min/avg/max = 6.555/10.093/27.021 ms
root@freescale /ecp5com/demos/comms_demos$
```

Figure 3: Network connection verification

Do the same verification on the other side (DAC board detected from ADC side):

```
> ping 192.168.2.224
```

6 Ordering Information

Please contact us via email contact@mikroprojekt.hr about item availability and ordering details.

7 Technical Support Assistance

Basic technical product support is free of charge and available via e-mail to all Mikroprojekt customers, whether they are evaluating or have purchased a Mikroprojekt product.

Basic technical support can be requested by sending an e-mail to support@mikroprojekt.hr

Our engineers will reply to your request within 2 working days.

Additionally, Mikroprojekt offers to its customers a premium support package, allowing them to be directly supported by Mikroprojekt engineers. The premium support package consists of 10 hours of live, online support, including:

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- Instant Messaging Support
- TeamViewer VNC Interventions.

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